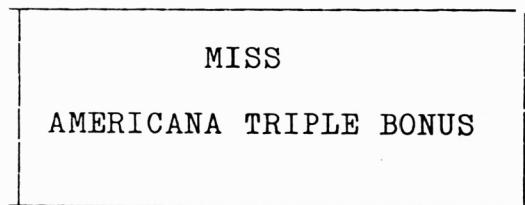


TECHNICAL MANUAL



Important note :

The printed circuits of the game remain exclusive possession of the drafter.

TECHNICAL MANUAL
MISS AMERICANA TRIPLE BONUS

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R E M A R K S

- Some drawings are spread over various pages, for instance, the one of PCB 28.
e.g. in zone C1 of drawing no. 112 one can find the sign INT RQST 1/C7. This means that the signal called INT RQST can be found back on sheet no. 1 of the drawings of PCB 28 and will be in zone C7 of those drawings.
- All the connectors of the game are indicated by J, followed by a number, the connections by flat cables are to be made wire to wire and the connecting ends have the same number J.
- Each connection by wire is indicated by a number; the flat cable-connections are called "LINK" (abbreviation LK) and the wire-connections are called "HARNESS" (abbreviation H).
- On most of the printed circuits with integrated circuits, the no. 1 pin of the IC is indicated by a circle beside the pin.
(See "COMPONENTS ASSEMBLY" N° 99 - PCB 28)
(See "COMPONENTS ASSEMBLY" N° 103 - PCB 32)
(See "COMPONENTS ASSEMBLY" N° 138 - PCB 44)
- The white nylon connectors (AMP MATE'N LOCK) are numbered.

CHAPTER 1 : MOUNTING THE BINGO

- Connect LK 4 (flat cable 34 wires) with J6 on PCB32
- Connect LK 5 (flat cable 16 wires) with J5 on PCB32
- Connect H3 (wires with white connector) with J27 on PCB43

1.1. Visual control before plugging in

- check if all plugs are put properly
- check if all I.C.s are put properly
- put the balls in the game
- check if PCB 47 (on top of PCB 28) is properly connected with J3

1.2. Plugging-in

The display should be lighted and the tilt-lamp should flash. (The shutter closes eventually)

In opposite case, the game must be switched off and the visual control restarted.

Note : if an error appears on the display, switch off and on again and the game should start.

If an error is appearing frequently, check the battery--tension (VVC on the CPU board PCB 28 : CHAPTER 11)

1.3. After assembling the game it is completely tested. Afterwards, the bingos are put for 24 hours in a 'TEST EPROM' position as life test. During these hours no defect may occur. Consequently, if problems occur on reception of the game, these emanate from the transport. (cable or components that loosen)

1.4. When the bingo operates one should verify all switches and lamps. (See CHAPTERS 4 and 10)

1.5. If everything is found O.K., adjust the play options with the dipswitches on PCB 42 and the reflex with the aid switches (See CHAPTER 3)

CHAPTER 2 : PRECAUTIONS

It is necessary to pay attention to certain precautions with regard to the printed circuits and the I.C.s.

2.1. Manipulation of the printed circuits

- put off the mains before touching the circuits.
- when switching off the matrix driver PCB 32 it is advisable to disconnect J4, because the filter capacitors are possibly charged
- the central computer unit PCB 28 B has a battery. This means that a part of it remains charged, even if the plugs are removed. This board may not be put on metal. (This causes complete destruction of the memories 5101 and almost always the diode D2/AAZ15 will break down.) One will not notice it right away as the battery is temporary still active. The result is a loss of credits, due to internal safety, when the credit-meter is reset.
- Never bridge over a fuse : use the correct one
- If transported separately, the boards should be packed in isolation material

2.2. Treatment of the I.C.'s

The I.C.s are very fragile, especially the pins. This can cause unexpected faults. In order to prevent these difficulties, one should pay attention to following rules :

2.2.1. Removal of the I.C.

If a pin is slightly bent, it will be bent completely when inserting the IC again. The only good way of removing an IC is with an "IC Extractor".

2.2.2. How to store the IC

After removing, the IC should be put on anti-static board (8155, 8085, 4049)

2.2.3. How to insert the IC

This is a very delicate matter. All pins should be vertical and well aligned.

One should insert an IC in such a way that no pin can be bent. Certain ICs are provided of 2 rows of pins, that are more distant of each other. In order to put them at the right distance, one should align them on a flat surface.

2.2.4. Static electricity

The semiconductors of the types MOS, CMOS, NMOS are very liable to static electricity through the large in- and outputresistance.

A spark of 1 millimeter needs a tension of 1000 Volts. The input or output of a memory MOS or e.g. 8085 is damaged by 25 or 50 static Volts.

The danger of static electricity is considerable when :

- synthetic carpet is used as floorcovering
- the climate is very warm and dry
- one can feel tension on the metal parts of the outside. In that case one should disconnect the bingo.
- One should never solder in a bingo that is still connected to the mains

CHAPTER 3 : SWITCHES FOR THE ADJUSTMENT
OF THE PLAY-OPTIONS

By means of 64 dipswitches it is possible to adjust the game-options.

One can find those switches on the dipswitch matrix PCB 42. They are subdivided in 8 groups of 8 switches. Each group is indicated with a letter from A to H and in each group the switches are numbered from 1 to 8.

Each dipswitch has two positions : position ON and position OFF on the switch itself.

3.1. The adjustment of credits versus coins

There are two coin acceptors.

Group C1 to C8 directs the right coin acceptor

Group B1 to B8 directs the left coin acceptor

The machines are adjusted as follows when leaving the factory :

Right coin acceptor : 3 coins give 5 credits on the REPLAY REGISTER

Left coin acceptor : 3 coins give 1 credit on the REPLAY REGISTER

With the help of the dipswitches one can adjust a coin rejector in such a way that 1 to 16 coins cause a transfer of 0 to 15 credits to the REPLAY REGISTER.

Acting this way, one can, for each coin acceptor adjust the number of coins (SW 1 to 4) in order to obtain a transfer of credits and with SW 5 to 8 one can determine the number of credits of such transfer.

3.1.1. Adjustment of coin acceptors

C4	C3	C2	C1	Right Coin Acceptor
B4	B3	B2	B1	Left Coin Acceptor
				<u>Number of Coins</u>
OFF	OFF	OFF	OFF	1 Coin
OFF	OFF	OFF	ON	2 Coins
OFF	OFF	ON	OFF	3 Coins
OFF	OFF	ON	ON	4 Coins
OFF	ON	OFF	OFF	5 Coins
OFF	ON	OFF	ON	6 Coins
OFF	ON	ON	OFF	7 Coins
OFF	ON	ON	ON	8 Coins
ON	OFF	OFF	OFF	9 Coins
ON	OFF	OFF	ON	10 Coins
ON	OFF	ON	OFF	11 Coins
ON	OFF	ON	ON	12 Coins
ON	ON	OFF	OFF	13 Coins
ON	ON	OFF	ON	14 Coins
ON	ON	ON	OFF	15 Coins
ON	ON	ON	ON	16 Coins

3.1.2. Adjustment of the value of the transfer of credits to the replay register

C8	C7	C6	C5	Right Coin Acceptor
B8	B7	B6	B5	Left Coin Acceptor
OFF	OFF	OFF	OFF	Number of Credits
OFF	OFF	OFF	ON	0 Credits
OFF	OFF	ON	OFF	1 Credits
OFF	OFF	ON	ON	2 Credits
OFF	ON	OFF	OFF	3 Credits
OFF	ON	OFF	ON	4 Credits
OFF	ON	ON	OFF	5 Credits
OFF	ON	ON	ON	6 Credits
OFF	ON	ON	ON	7 Credits
ON	OFF	OFF	OFF	8 Credits
ON	OFF	OFF	ON	9 Credits
ON	OFF	ON	OFF	10 Credits
ON	OFF	ON	ON	11 Credits
ON	ON	OFF	OFF	12 Credits
ON	ON	OFF	ON	13 Credits
ON	ON	ON	OFF	14 Credits
ON	ON	ON	ON	15 Credits

3.2. Adjustment of the reflex

3 different adjustments are possible that can influence the percentage TOTAL OUT/TOTAL IN of the game :

3.2.1. Adjustment of the "PLOTS"

Switch A5 in position "ON"

Will add "PLOTS", thus chances in that section of the reflex, which controls the score and other balls.

Switch A4 in position "ON"

Will add chances in that section of the reflex which controls the features and the selection.

3.2.2. Adjustment of the relation IN-OUT

A3	A2	A1	Level
OFF	OFF	OFF	1 Most Liberal
OFF	OFF	ON	2
OFF	ON	OFF	3
OFF	ON	ON	4
ON	OFF	OFF	5
ON	OFF	ON	6
ON	ON	OFF	7
ON	ON	ON	8 Most conservative

3.2.3. Stop of the Reflex

There is a possibility to block the reflex, if F7 is put in position "ON".

Evidently, the regulating action of the reflex will disappear, which is not recommendable. The normal position of F7 is thus "OFF".

3.3. Adjustment of features and extra balls

The principle remains the same : if a dipswitch is put on "ON", chances are added to a spotting or mixer, thus to a feature.

A8	:	Corners
E1	:	Corners
E7	:	Extra Card (normal = ON) - OFF = 50 %
E8	:	Any 2
F1	:	Any 3
E3	:	4 Stars as green
E2	:	4 Stars as green
F2	:	Extra Ball
F3	:	Extra Ball
F4	:	Extra Ball
F5	:	Extra Ball

3.4. Adjustment of the option "32 Points"

When the reflex is very conservative, long periods of putting credits may give nothing to the player. To avoid this, an internal system will give an automatic step to the selection (or to the Extra Ball) at the 32nd point, consecutively played.

- G4 on "ON" gives this option for the selection
- G2 on "ON" gives this option for the Extra Balls

3.5. Option Rest (Knock-off)

Normal function : Dipswitch F8 = OFF. After cutting off and switching on the power, the bingo will automatically deduct the points from the REPLAY REGISTER and add them to the TELEPHONE OUT counter.

If the Dipswitch is in position ON, the credits are kept on the REPLAY REGISTER. In order to knock them off, one should use the special button on the telephone (See CHAPTER 4)

3.6. Option 2nd Mixer 2

The machine has a complete 2nd mixer 2 which gives reduced chances to the score and Extra Balls (in fact to the influence of the features on Score and Extra Balls).

The normal position is G5 on "OFF"

If G5 is on "ON", the mixer 2 is activated.

3.7. Option speed of the game

The time of the start-cyclus can be adjusted (= speed of control unit motor) between 2 values :

- G3 = ON : FAST (approximately 0,5 sec)
- G3 = OFF : SLOW (approximately 0,75 sec)

(for an adjustment of the internal request of 2 milliseconds of a period).

3.8. Option Self Test of the Memories

Normal position H1 = OFF

If put on "ON", the machine continues to function, but very slowly, because it will test the memories. This is used in the factory for the "BURN" test with a 24 hours function; it can also be used in the workshop.

If a memory is found to be defective (or the program does not "turn" properly), the display (replay register) will indicate an error code (see chapter 7).

3.9. Important

All the non-cited dipswitches are to be on position OFF.

3.10. Control of the dipswitches on PCB 42

To verify the dipswitches, the machine has to be put on "SEEINSIDE" at the symbolic address <Dipswitch> (see symbolic addresses, chapter 16). The display will show the state of group D. On the following 8 addresses, it will show :

DIPSW	Dipsw D
DIPSW +1	Dipsw C
DIPSW +2	Dipsw B
DIPSW +3	Dipsw A
DIPSW +4	Dipsw E
DIPSW +5	Dipsw F
DIPSW +6	Dipsw G
DIPSW +7	Dipsw H

In order to get a complete test, proceed as follows :

3.10.0. Disconnect J5, coming from the body.

1	2	3	4	5	6	7	8
ON	OFF	ON	OFF	ON	OFF	ON	OFF

The display must read 55. If not, there is a fault.

3.10.2. Put all the switches in opposite position

1	2	3	4	5	6	7	8
OFF	ON	OFF	ON	OFF	ON	OFF	ON

The display should read AA (the signal) if not, there is a fault.

3.10.3. Put the 8 dipswitches of the group on ON. The display should read FF (which means extinction).

3.10.4. Put the 8 dipswitches of the controlled group on OFF. The display should read 00.

3.11. Factory Dipswitch Adjustment (level 3)

1 = ON / 0 = OFF

	8	7	6	5	4	3	2	1
A	1	1	0	1	1	0	1	0
B	0	0	0	1	0	0	1	0
C	0	1	0	1	0	0	1	0
D	0	0	0	0	0	0	0	0
E	1	1	0	0	0	1	1	0
F	0	.0	0	0	0	1	1	1
G	0	0	0	0	1	1	0	0
H	0	0	0	0	0	0	0	0

3.12. Important Notice

- The MISS AMERICANA TRIPLE BONUS with a hardware random PCB 74.
- When PCB 74 is connected with J3 on PCB 28, all dipswitches D are to be in the OFF position (in fact their position is of no importance anymore).
- Without PCB 74 being connected, the position of the dipswitches D is as follows :

8	7	6	5	4	3	2	1
ON	ON	OFF	OFF	ON	OFF	ON	OFF

- With PCB 74 the variability around the point of the reflex is more limited than without.

CHAPTER 4 : CONNECTION OF THE REMOTE-CONTROL (Telephone)

4.1. General description of the remote control

The telephone consists of 2 boards :

- PCB 35 = board in the bingo
- PCB 36 = board in the telephone box

The latter is delivered together with each machine and has to be mounted in a telephone box, which has push-buttons and 2 totalising counters TEL IN and TEL OUT (RESET /KNOCK-OFF). Connection schemes can be found in this manual.

Several options are possible, depending on the way in which PCB 35 and 36 are connected.

4.2. Regular version : with 7 wires

In this version the connection between remote control box (PCB 36) and bingo (PCB 35) is made by a cable with 7 wires :

1. TEL A
2. TEL B
3. TEL C
4. TEL D
5. COMMON WIRE (Switches and Counters)
6. Pulses Telephone In
7. Pulses Telephone Out

This connection gives following possibilities :

- 13 credit values
- knocking-off by pushing simultaneously on the TEL D and 7 (and pulses TEL OUT) button

4.3. Shortened version : with 6 wires

The TLF D is not used anymore.

- knocking-off through the Telephone box is not possible
- Only 7 instead of 13 credit values are obtainable

The six wires are the following :

1. TEL A
2. TEL B
3. TEL C
4. COMMON WIRE
5. PULSES TELEPHONE IN
6. PULSES TELEPHONE OUT

4.4. Version with 5 wires

Same as version 4.3. TEL C is not connected. Only 3 values on the telephone are available.

4.5. Option counters 50 VAC - 6 or 12 VDC

The telephone board in the bingo is fitted for realising different bridges.

That is the reason why in the TEL Box 50 VAC counters or DC 6V or 12 V counters can be used. We recommend the use of counters 6 VDC (with resistance equal to wire resistance value) in serie with the 2 counters TEL IN and OUT

Telephone Box board changes also, depending on the choice between 50 VAC or 6 or 12 VDC. We deliver those for 50 VAC because this is the most common voltage for the counters.

Following possibilities are on hand :

- 50 VAC)
- 6 VDC + serie-resistance) tension for the counters
- 12 VDC)
- cable with 7 wires (13 credit values)
- cable with 6 wires (7 credit values)
- cable with 5 wires (3 credit values)

4.6. The LED-codes on the internal telephone box PCB 35

It indicates the binary code of the TEL buttons and enables to check the correctness of the connections. The proportion between the code and value depends on the program type.

	LED D	LED C	LED B	LED A
Button 1	-	-	-	ON
Button 2	-	-	ON	-
Button 3	-	-	ON	ON
Button 4	-	ON	-	-
Button 5	-	ON	-	ON
Button 6	-	ON	ON	-
Button 7	-	ON	ON	ON

Led D will only light up when pushing the D button. When knocking off all LEDs will be lit.

4.7. Knock-off

If one wants to obtain the knock-off function thru the telephone, using only one single button, one should provide a switch with two circuits.

- one closing the circuits of D
- a second one, closing the circuit of switch 7

CHAPTER 5 : THE ADJUSTMENT OF THE REFLEX

5.1. Reading of the reflex

- Connect Service Box SB 1 (*)
- Switch SV1 in permanent "ON" position. The display will read the address of <RFX> = 4009
- Switch on SV4 (= SEEBUT). The display will get divided in 2 parts. The 2 left side numbers which are flashing will give you the real position of the reflex and the right side numbers will give you the position of the reflex that you want.

5.2. Writing or modifying the reflex

- Proceed as above
- By means of SV2 (+ + 1 BUT) the right side part can be brought at the requested value + 1.
(e.g. if value 9 is wanted, write 10)
- Start a game with the red button : the left side part will become the same as the right side. (In the example = 10)
- Start a second game. The two parts will go to 9 (= the wanted value).
- With a faulty handling (e.g. write a number higher than 31) the starting of the game will cancel the manoeuvre.

5.3. Other adjustments of the reflex

See 3.2.

5.4. Replacement of Central Processor Unit PCB 28 B

The reflex is a non-volatile address in the memory, situated in the two I.C.'s 5101 on PCB 28 B.

If this board is replaced, the two ICs should have to be taken out of the first one, and put back on the second.

This is important since the two ICs contain all counters as well as the reflex.

CHAPTER 6 : SB1 and SB2

6.1. SB1

Has to be connected with J29, situated at the front of the machine, near the connection of the door-wires. The connector is type AMP MATE'N LOCK.

6.1.1. Use of SB1

SV5	: Testing of the outputs
SV6	: Testing of the inputs
SV1 - SV2 - SV3 - SV4	: Entry to service program "SEEIN-SIDE", authorising reading or writing of any memory position.

6.2. SB2

- To test the 2 contact matrixes, which are the contact matrix of the game and the matrix of the dipswitches.
- To perform a hardware-test of these matrixes, meaning to locate a deficiency found through e.g. the input-test.
- To test the flat cables with 16 conductors (only with short-circuits).

6.3. Other Servicing Supports

- Testing the memories through Dipswitch H1 (see chapter 3)
- SB3 : flat cables-tester
- SB4 : Test equipment for in and output of PCB 28

CHAPTER 7 : ERROR CODES

7.1. If the machine itself detects a failure, its normal function will stop and it will enter into a part of the program which will display a signal-code, indicating the error.

Two kinds of tests can be distinguished :

- a first test, effected at the moment of connecting the machine, and thus only once.
- another series of tests, effected continuously

7.2. Anyway, a blocking position is inevitable and can only be eliminated by cutting off the powerline. If the defect lasts, the machine will go again to an error-code.

7.3. Please note that the micropocessor can be in error and give a wrong error-code.

If the microprocessor states an error-code, it ascertains a defect at some part of the machine. It is possible that a mistake occurs in the indication of the component. Consequently the error-code is wrong.

7.3.1. An error-code does not always mean that a certain element is defective.

7.3.2. On the contrary, it can mean that the microprocessor cannot fulfill the test successfully. The reason for this evil is to be determined by the technician.

7.3.3. One should not throw away immedately a certain component , because the defect code can derive from an other one.

7.3.4. How to act? Just replace the indicated component by a new one and repeat the test. If the error-code disappears, the microprocessor was not mistaken. If the error-code remains, look further.

7.3.5. The repair has been successful

- if the game starts up again
- if all normal tests do not indicate an error-code anymore
- if one can play again

7.3.6. Typical example

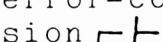
The voltage supply of the microprocessor board PCB 28 (+ 5V) is very important. Imagine that a diode or a condenser is defective and a strong wave exists on this tension : the microprocessor will

- function poorly, even during tests
- indicate the memory as defective, even if it is in order

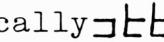
In this particular case, the sequence of the tests is very important. Most probably, the first test by the microprocessor will not be executed.

7.4. Sequence of the tests executed when connecting the power-line and the emanating error-codes..

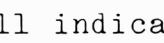
7.4.1. Test of the RAM memories

The RAM memories are subdivided in 4 groups. The error-code AEEA corresponds with the graphic version  and shows the first group of the RAM being defective.

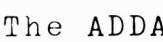
Here, the memories 5101 (22 pins) are concerned, of which one of both could be defective, without being able to determinate which one.

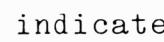
Error-code BEEB (graphically ) will indicate an error in the test of the I.C. 8155 Q2 (40 pins)

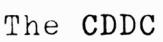
Code CEEC () will indicate the I.C. 8155 Q3

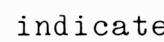
Code DEED () will indicate the I.C. 8155 Q4

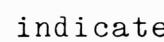
7.4.2. Test of the EPROM memories

The ADDA () code indicates the Eeprom memory in position A.

The BDDB () code indicates the memory in position B.

The CDDC () code indicates the memory in position C.

The DDDD () code indicates the memory in position D.

The EDDE () code indicates the memory in position E.

7.4.3. Non-volatility test

Power is permanently supplied to the contents of the RAM memories 5101 by a battery (3 x 1,2 V or A x 3,6 V). These contents are very important (e.g. the value of the REPLAY REGISTER and the different counters).

This justifies the test executed by the microprocessor, verifying whether the contents are valid. If the microprocessor cannot accept the value, defect code AAAA will appear, or graphically ~~CCCC~~

This will always occur when :

- memories 5101 have been replaced
- a bad EPROM has been replaced
- the battery or diode (AAZ 15) in serie with the battery is defect. (e.g. the microprocessor board has been put on metallic parts during transportation)

7.4.4. Accumulator test and diode AAZ 15

With a voltmeter, one can measure the tension between the mass and Pin 22 on one of both Ram memories 5101 : it should be between 2,6 and 4 Volts.

This can be realised by disconnecting the microprocessor board or the bingo itself. If the defect remains, diode AAZ 15 is defective, (resulting from a bad handling of the microprocessor board PCB 28B), or the battery is defective, (which can be measured directly on the battery).

7.5. Tests executed during the game

Large tests are involved that control in a severe way the REPLAY REGISTER. When the code BBBB appears (ココココ), the microprocessor registered an anomaly in the value of the REPLAY REGISTER. This can be due to anything whatsoever, included cheating.

The microprocessor will not take the risk to give away credits and will secure itself and cancel the contents of the Replay Register.

Note : The amount of credits which has disappareared due to a failure can be reconstructed by means of a calculation on the mechanical counters. This is a better procedure than having 1000 credits on the Replay Register without any reason whatsoever.

7.6. The code CCC (CCC) indicates that the microprocessor has executed the order FF, which means that it has gone out of program. In most of the cases this is due to a defective EPROM, or to the Random Number Generator or to a wrong tension in a section.

If there are problems with the voltage it is recommended to use a stabilisor

CHAPTER 8 : IN- AND OUTPUT MATRIXES

A more technical description will be given later. First we will handle the basic principles.

8.1. Introduction

The denominations in- and output refer to the microprocessor board.

- Input : an information read by the microprocessor on the contacts.
- Output : data sent from the microprocessor to the bingo, which are :
 - the ignition of a lamp
 - the start-up of a motor
 - a relay to be energised
 - the addition of a credit to the replay counter
 - the ignition of a LED on the display

8.2. The Inputs :

There are 128 switches in the game (including the dip-switches). In order to bring these independantly to the microprocessor board one would need 128 wires. Now we use the principle of the matrix which only needs $8 + 8 + 8 = 24$ wires. The microprocessor can interrogate the 128 contacts of the game cyclically ($128 \times (8 \times 2) \times 8$)

The inputs are divided in 2 matrixes of 8×8

8.2.1. The input matrix interrogating all the switches of the body and playfield

The matrix is represented by 8 columns (abbreviation : 8 col.) numbered from col 1 to col 8 and by 8 rows, numbered from row 1 to row 8. One flat cable, coming from matrix driver connector J5 on matrixdriver PCB32 will transmit these 16 lines (8 col + 8 row) to the game.

The boards PCB 33 Body Split, PCB 38 and PCB 46/1 to 5 will send the signals to the different contacts of the machine. In serie with each contact there is a diode IN 4148 which unables interaction between the contacts.

8.2.2. The input matrix which includes the dipswitches

PCB42 consists of 8 groups of 8 contacts, called dipswitches. This matrix is read the same way as the previous matrix, with the same columns. Only the rows are different : Row 9 to Row 16, generated by 74145 which is activated when "SCAN D" is on level 1.

8.3. Output matrix of the lamps

The lamps are built in a matrix 8 x 18, good for 144 lamps. Each lamp has one serial diode IN4003. The rows are numbered from X1 to X8 and the columns from Y1 to Y18.

The function principle of the lamps is the following :

One provides an X-row of 20 V (+ VM) and makes one or more Y columns conductive. The lamp or lamps on the intersections of the X-row with the conductive Y-columns, will light up. Each 2 milliseconds another X-row on the microprocessor will be energised and if needed, also other or same Y-columns.

As the lamps receive only 1 pulse during 1/8 in time, they will light up normally, due to higher voltage.

8.4. What to retain from the foregoing?

The contacts are put on the intersections of the matrix, with each time one diode in series.

Each contact can be found on the intersection of a Col-line and a Row-line (COL and ROW).

There are 8 COLUMNS and 16 ROWS

The contacts from the game only use the Rows 1 to 8.

The dipswitches use Rows 9 to 16, but are read by same Columns. (In case of defective wires, mutual influence is possible)

Also the lamps on the intersections of a matrix are connected with one diode in series.

One can always find them on the intersections of one of the 8 rows X1 - X8, (they supply the voltage VM) and one of the 8 columns Y1 - Y8 (which supply the mass)

8.5. The division of the switches in the matrix is described in CHAPTER 9.

CHAPTER 9 : TEST OF THE OUTPUTS

Switch SV5 on the service box SB1 and the machine will enter into an automatic output-testprogram : each output has a number from 1 to 156, which will appear on the display.

The switches SV1 and SV3 (+1 and -1) will allow you to increase or decrease the above-mentioned number.

The list hereunder gives you the xy location in the matrix of the multiplex outputs (lamps). A standard abbreviation has been given to each output.

Note that some numbers are not used because there is no connection made for in the matrix.

This test can disturb the "at ease" position of different motors, especially of the magic lines-motors; they should be put correctly by igniting ABCDE and by moving them with the buttons ABCDE.

List of the Outputs

NBR	ROW	COL	ABBREVIATION	NAME AND REMARKS
1	1	1	A	Magic Lite "A" on Main Card
2	1	2	B	Magic Lite "B" on Main Card
3	1	3	C	Magic Lite "C" on Main Card
4	1	4	D	Magic Lite "D" on Main Card
5	1	5	E	Magic Lite "E" on Main Card
6	1	6	AA	Magic Lite "AA" on Main Card
7	1	7	BB	Magic Lite "BB" on Main Card
8	1	8	CC	Magic Lite "CC" on Main Card
9	1	9	DD	Magic Lite "DD" on Main Card
10	1	10	EE	Magic Lite "EE" on Main Card
11	1	11	RED 4	Lite Red Score 3 In Line = 4
12	1	12	RED 8	Lite Red Score 3 In Line = 8
13	1	13	RED 16	Lite Red Score 3 In Line = 16
14	1	14	RED 32	Lite Red Score 3 In Line = 32
15	1	15	RED 64	Lite Red Score 3 In Line = 64
16	1	16	RED 96	Lite Red Score 3 In Line = 96
17	1	17	RED 128	Lite Red Score 3 In Line = 128
18	1	18	RED 160	Lite Red Score 3 In Line = 160
19	2	1	F	Magic Lite "F" 2nd Line Main Card
20	2	2	G	Magic Lite "G" 2nd Line Main Card
21	2	3	H	Magic Lite "H" 2nd Line Main Card
22	2	4	I	Magic Lite "I" 2nd Line Main Card
23	2	5	J	Magic Lite "J" 2nd Line Main Card
24	2	6	FF	Magic Lite "FF" 2nd Line Main Card
25	2	7	GG	Magic Lite "GG" 2nd Line Main Card
26	2	8	HH	Magic Lite "HH" 2nd Line Main Card
27	2	9	II	Magic Lite "II" 2nd Line Main Card
28	2	10	JJ	Magic Lite "JJ" 2nd Line Main Card
29	2	11	YELLOW 4	Lite Yellow Score 3 In Line = 4
30	2	12	YELLOW 8	Lite Yellow Score 3 In Line = 8
31	2	13	YELLOW 16	Lite Yellow Score 3 In Line = 16
32	2	14	YELLOW 32	Lite Yellow Score 3 In Line = 32
33	2	15	YELLOW 64	Lite Yellow Score 3 In Line = 64
34	2	16	YELLOW 96	Lite Yellow Score 3 In Line = 96
35	2	17	YELLOW 128	Lite Yellow Score 3 In Line = 128
36	2	18	YELLOW 160	Lite Yellow Score 3 In Line = 160
37	3	1	K	Magic Lite "K" 3rd Line Main Card
38	3	2	L	Magic Lite "L" 3rd Line Main Card
39	3	3	M	Magic Lite "M" 3rd Line Main Card
40	3	4	N	Magic Lite "N" 3rd Line Main Card
41	3	5	O	Magic Lite "O" 3rd Line Main Card
42	3	6	KK	Magic Lite "KK" 3rd Line Main Card
43	3	7	LL	Magic Lite "LL" 3rd Line Main Card
44	3	8	MM	Magic Lite "MM" 3rd Line Main Card
45	3	9	NN	Magic Lite "NN" 3rd Line Main Card
46	3	10	OO	Magic Lite "OO" 3rd Line Main Card
47	3	11	GREEN 4	Lite Green Score 3 In Line = 4

NBR	ROW	COL	ABBREVIATION	NAME AND REMARKS
48	3	12	GREEN 8	Lite Green Score 3 In Line = 8
49	3	13	GREEN 16	Lite Green Score 3 In Line = 16
50	3	14	GREEN 32	Lite Green Score 3 In Line = 32
51	3	15	GREEN 64	Lite Green Score 3 In Line = 64
52	3	16	GREEN 96	Lite Green Score 3 In Line = 96
53	3	17	GREEN 128	Lite Green Score 3 In Line = 128
54	3	18	GREEN 160	Lite Green Score 3 In Line = 160
55	4	1	P	Magic Line 4th Line Main Card
56	4	2	Q	Magic Line 4th Line Main Card
57	4	3	R	Magic Line 4th Line Main Card
58	4	4	S	Magic Line 4th Line Main Card
59	4	5	T	Magic Line 4th Line Main Card
60	4	6	PP	Magic Line 4th Line Main Card
61	4	7	QQ	Magic Line 4th Line Main Card
62	4	8	RR	Magic Line 4th Line Main Card
63	4	9	SS	Magic Line 4th Line Main Card
64	4	10	TT	Magic Line 4th Line Main Card
65	4	11	WHITE 4	Lite White Score 3 In Line = 4
66	4	12	WHITE 8	Lite White Score 3 In Line = 8
67	4	13	WHITE 16	Lite White Score 3 In Line = 16
68	4	14	WHITE 32	Lite White Score 3 In Line = 32
69	4	15	WHITE 64	Lite White Score 3 In Line = 64
70	4	16	WHITE 96	Lite White Score 3 In Line = 96
71	4	17	WHITE 128	Lite White Score 3 In Line = 128
72	4	18	WHITE 160	Lite White Score 3 In Line = 160
73	5	1	U	Magic Lite 5th Line Main Card
74	5	2	V	Magic Lite 5th Line Main Card
75	5	3	W	Magic Lite 5th Line Main Card
76	5	4	X.	Magic Lite 5th Line Main Card
77	5	5	Y	Magic Lite 5th Line Main Card
78	5	6	UU	Magic Lite 5th Line Main Card
79	5	7	VV	Magic Lite 5th Line Main Card
80	5	8	WW	Magic Lite 5th Line Main Card
81	5	9	XX	Magic Lite 5th Line Main Card
82	5	10	YY	Magic Lite 5th Line Main Card
83	5	11	NC	Not Connected
84	5	12	BBOX Y	Lite Bonus Box Yellow
85	5	13	BONAR 1Y	1st Bonus Arrow Yellow
86	5	14	BONAR 2Y	2nd Bonus Arrow Yellow
87	5	15	BONAR 3Y	3rd Bonus Arrow Yellow
88	5	16	BONAR 4Y	4th Bonus Arrow Yellow
89	5	17	BONAR 5Y	5th Bonus Arrow Yellow
90	5	18	BONMAD Y	Bonus Yellow Made
91	6	1	EB BOX	Lite Extra Ball Box
92	6	2	1ST	Lite FIRST
93	6	3	1 EXTRA	Lite EXTRA
94	6	4	1 BALL	Lite BALL
95	6	5	2ND	Lite SECOND
96	6	6	2 EXTRA	2 EXTRA

NBR	ROW	COL	ABBREVIATION	NAME AND REMARKS
97	6	7	2 BALL	Lite 2 BALL
98	6	8	3RD	Lite THIRD
99	6	9	3 EXTRA	Lite 3 EXTRA
100	6	10	3 BALL	Lite 3 BALL
101	6	11	SND 1	SOUND COILS N° 1
102	6	12	BBOX G	Lite Bonus Box Green
103	6	13	BONAR 1G	1st Bonus Arrow Green
104	6	14	BONAR 2G	2nd Bonus Arrow Green
105	6	15	BONAR 3G	3rd Bonus Arrow Green
106	6	16	BONAR 4G	4th Bonus Arrow Green
107	6	17	BONAR 5G	5th Bonus Arrow Green
108	6	18	BONMAD G	Bonus Green Made
109	7	1	BBOX 1W	Lite Bonus Box White
110	7	2	BONAR 1W	1st Bonus Arrow White
111	7	3	BONAR 2W	2nd Bonus Arrow White
112	7	4	BONAR 3W	3rd Bonus Arrow White
113	7	5	BONAR 4W	4th Bonus Arrow White
114	7	6	BONAR 5W	5th Bonus Arrow White
115	7	7	BONMAD N	Bonus White Made
116	7	8	ANY 2	Lite ANY 2 for OK
117	7	9	ANY 3	Lite ANY 3 for OK
118	7	10	SEL 1	1st Arrow of Selection ABCDE
119	7	11	SEL 2	2nd Arrow of Selection ABCDE
120	7	12	SEL 3	3rd Arrow of Selection ABCDE
121	7	13	SEL 4	4th Arrow of Selection ABCDE
122	7	14	SELAB	Lite AB of Selection
123	7	15	SEL C	Lite C of Selection
124	7	16	SEL D	Lite D of Selection
125	7	17	SEL E	Lite E of Selection
126	7	18	-----	Not Connected
127	8	1	CORNER	Lite CONERNER
128	8	2	4 STAR	Lite 4 STARS AS GREEN
129	8	3	EX CARD	Lite EXTRA CARD
130	8	4	ROLOVR	Lite ROLLOVER RED
131	8	5	ROLOVY	Lite ROLLOVER YELLOW
132	8	6	N/C	Not Connected
133	8	7	LTIILT	Lite TILT
134	8	8	N/C	Not Connected
135	8	9	BEF 4	Lite Select before 4th Ball
136	8	10	BEF 5	Lite Select before 5th Ball
137	8	11	SELNOW	Lite SELECT NOW
138	8	12	OKMAD	OK MADE
139	8	13	N/C	Not Connected
140	8	14	RED 192	Lite Red Score 3 In Line 192
141	8	15	YELLOW 192	Lite Yellow Score 3 In Line 192
142	8	16	WHITE 192	Lite White Score 3 In Line 192
143	8	17	GREEN 192	Lite Green Score 3 In Line 192
144	8	18	N/C	Not Connected
145	-	--	TLF OUT	TELEPHONE OUT (Knock-off)

NBR	ROW	COL	ABBREVIATION	NAME AND REMARKS
146	-	-	TLF IN	TELEPHONE IN Counter
147	-	-	TOT OUT	TELEPHONE OUT Counter
148	-	-	TOT IN	TOTAL IN Counter
149	-	-	MAG MOT A	MAGIC MOTOR Line A
150	-	-	MAG MOT B	MAGIC MOTOR Line B
151	-	-	MAG MOT C	MAGIC MOTOR Line C
152	-	-	MAG MOT D	MAGIC MOTOR Line D
153	-	-	MAG MOT E	MAGIC MOTOR Line E
154	-	-	CAS HB	Credit Counter
155	-	-	MOT LIF	Balllifter Motor
156	-	-	MOTSHU	Playfield Motor

CHAPTER 10 : TEST OF THE INPUTS

These inputs are the switches of the body and the playfield.

The dipswitches of PCB 42 are also inputs, but are not considered in this chapter (see chapter 3)

10.1. Switch SV5 on the SB1-Box : the outputs-test is entered into with SV2 and SV3. Bring the rank-number at 155. (Use the "-1").

10.2. Bring SV5 in neutral position and tilt the game. The playfield will colse.

10.3. Switch SV6 : an automatic test-program of the switches of body and playfield will be activated.

Identical to the outputs, a rank-number will be given to each switch (from 1 to 62).

The list hereunder will give the exact location of each switch in the matrix of Rows and Columns.

The rank-number will be displayed and will stay put if only one switch is closed. If more switches are closed, all the rank-numbers of the closed switches will appear for a short while.

- With the balls removed and the game tilted, all the switches are to be opened and the display is to be clear.
- For testing, activate the switches one by one : the display has to show the rank-number of the activated switch.

10.4. By switching SV6 to the normal position, the game goes to the normal program.

10.5. "THROUGH SW." are numbered from THROUGH 1 to THROUGH 7 from the right to the left and THROUGH 0 is located under the Balllifter.

10.6. List of the entries

NBR.	ROW	COL.	ABBREVIATION	DENOMINATION + FUNCTION OF THE SWITCH
1	1	1	HOLE 1	Hole Nbr 1 on playfield
2	1	2	HOLE 2	Hole Nbr 2 on playfield
3	1	3	HOLE 3	Hole Nbr 3 on playfield
4	1	4	HOLE 4	Hole Nbr 4 on playfield
5	1	5	HOLE 5	Hole Nbr 5 on playfield
6	1	6	HOLE 6	Hole Nbr 6 on playfield
7	1	7	HOLE 7	Hole Nbr 7 on playfield
8	2	1	HOLE 8	Hole Nbr 8 on playfield
9	2	2	HOLE 9	Hole Nbr 9 on playfield
10	2	3	HOLE 10	Hole Nbr 10 on playf.
11	2	4	HOLE 11	Hole Nbr 11 on playf.
12	2	5	HOLE 12	Hole Nbr 12 on playf.
13	2	6	HOLE 13	Hole Nbr 13 on playf.
14	3	1	HOLE 14	Hole Nbr 14 on playf.
15	3	2	HOLE 15	Hole Nbr 15 on playf.
16	3	3	HOLE 16	Hole Nbr 16 on playf.
17	3	4	HOLE 17	Hole Nbr 17 on playf.
18	3	5	HOLE 18	Hole Nbr 18 on playf.
19	3	6	HOLE 19	Hole Nbr 19 on playf.
20	3	7	HOLE 20	Hole Nbr 20 on playf.
21	3	8	HOLE 21	Hole Nbr 21 on playf.
22	4	1	HOLE 22	Hole Nbr 22 on playf.
23	4	2	HOLE 23	Hole Nbr 23 on playf.
24	4	3	HOLE 24	Hole Nbr 24 on playf.
25	4	4	HOLE 25	Hole Nbr 25 on playf.

<u>NBR</u>	<u>ROW</u>	<u>COL</u>	<u>ABBREV.</u>	<u>NAME + FUNCTION</u>
26	1	8	SHUTTER	Switch open if ball return panel is closed
27	2	7	GATESW	Switch on top of playfield where ball enters the playfield
28	2	8	COSHUT	Carry over from the shutter motor
29	4	5	ROLRSW	Red rollover on the playfield
30	4	6	ROLYSW	Yellow rollover on the playfield
31	4	7	ALLEYSW	Switch for ballshooter
32	4	8	SW 48	Not connected
33	5	1	TRG 1	Through Switch 1
34	5	2	TRG 2	Through Switch 2
35	5	3	TRG 3	Through Switch 3
36	5	4	TRG 4	Through Switch 4
37	5	5	TRG 7	Through Switch 7
38	5	6	COLIFT	Carry over balllifter
39	5	7	PULSLI	Restcontact balllifter
40	5	8	MANLIF	Manual balllift button
41	6	1	R BUT	R Button
42	6	2	X BUT	X Button
43	6	3	N/C	Not Connected
44	6	4	DOORSW	Doorsw (closed when door is open)
45	6	5	TRG	Balllifter switch of Through Switch 0
46	6	6	N/C	Not Connected
47	6	7	N/C	Not Connected
48	6	8	N/C	Not connected
49	7	1	TIILT SW	Tilt contact
50	7	2	REDBUT	Red doorbutton
51	7	3	YELBUT	Yellow doorbutton
52	7	4	A BUT	A Button Magic Lines
53	7	5	B BUT	B Button Magic Lines
54	7	6	C BUT	C Button Magic Lines
55	7	7	D BUT	D Button Magic Lines
56	7	8	E BUT	E Button Magic Lines
57	8	1	COIN 1	Coin switch 1 on the door
58	8	2	COIN 2	Coin switch 2 on the door
59	8	3	SV1	On SB1 : Service Switch
60	8	4	SV2	On SB1 : + 1 Button
61	8	5	SV3	On SB1 : - 1 Button
62	8	6	SV4	On SB1 : See Button
63	8	7	SV5	On SB1
64	8	8	SV6	On SB1

10.7. Switch-test of Magic Motors

Each magic motor has 2 switches activated through a wheel with 3 notches. These switches are searched through ROW1 to ROW5 and read through 2 special columns, called SW RIGHT and SW LEFT. The corresponding Optocouplers on PCB 28B are Q35 and Q34. The switches are opened at the notches; the 3 positions of each strip correspond with the following situations of the switches.

Position of the wheel	SW L	SW R
Neutral Position	OFF	OFF
Left	ON	OFF
Right	OFF	ON
Moving = Intermediate Positions = carry over function	ON	ON

For the left side group ACE, the SW A is in the back and for the right side group BD, the SW A is in the front.

To test these switches, use the SB1 and "SEEINSIDE".

Proceed as follows :

- 1) Switch SV1 to go to "SEEINSIDE"
- 2) Put the address indicator on <MLAST>
- 3) Switch SV4 to get a display. The right side of the display will show :
 - 00 = Wheel in neutral position (SW L & R OFF)
 - 01 = Wheel in left position (SW L ON)
 - 02 = Wheel in Right position (SW R ON)
 - 03 = wheel moving (SW L & R ON)
- 4) Set indicator on +1 and go back for strip B
- 5) Idem for strips C, D, E

If an error is found, verify or replace the following components : Microswitches H9, H8, J28L, J28R, J9, PCB34, LK8, J1, LK1, Q34 & Q 95 on PCB28B, Q3 on PCB 28B

Reminder :

H = Harness
LK = Connection
J = Connector
Q = IC
PCB = Board

CHAPTER 11 : TEST OF THE POWER SUPPLY

First study the diagram of PCB 043. Then examine power supply card PCB 43D :

- It contains 3 plugs :
 - J27 : entries from the transformer
 - J26 : exits to matrix driver PCB 32B (J4)
 - J42 : filtercapacities.
- It contains also 4 rectifier bridges, rectifying 4 voltages simultaneously :
 - Power supply voltage for the VCC
 - + 12 V common
 - + V Multiplex (+ VM)
 - floating 12 V

Those 4 voltages have a + and a -. The first three have a common ground (minus). GND IC = GROUND INTEGRATED CIRCUIT, forming the mass of the electronic card, consisting of computer PCB 28, matrix PCB 32 and display card PCB 91

Test of those 3 voltages is effected with the negative of the voltmeter on the common negative wire of the 4 thick filtercapacities.

11.1. Test of the power supply voltage for the VCC on PCB 43D :

+ testpoint on fuse F2
This voltage should fluctuate between +9 and +14 Volt DC.
Typical voltage for PCB 43D = 9,5 V.

11.2. Test of the Common 12V :

+ testpoint on fuse F7 on power supply card PCB 43D.
The value read should fluctuate between +12 and +15;
mostly 13,5 V.

11.3. Test of the lamp voltage VM :

+ testpoint : on fuse F3 of power supply card PCB 43D.
The value shown should fluctuate between 20 and 28 Volt DC,
depending from the number of lamps lightning.

11.4. Test of VCC :

The VCC 1 is the power supply voltage of computer card PCB 28.

This voltage is diverted from the power supply voltage of the VCC.

Testpoints + on TP1 of matrix driver PCB 32.
- on TP3 of matrix driver PCB 32

The value should be between 4,75 V and 5,25 V. The best is to obtain exactly 5V.

11.5. Test of VCC 2 :

VCC 2 is the + 5V voltage for the IC on the matrix driver card PCB 32 and the display card PCB 91.

VCC 2 is diverted via a voltage stabilizer LM 309K, Q12 on the card itself.

Testpoints + on TP2 of matrix driver PCB 32
- on TP3 of matrix driver PCB 32

The value should be 4,75 and 5,25 VDC. The best is 5V.

11.6. Test of the floating + 12 V :

This floating voltage has a common point with the 50 VAC 1 on the transformer

Testpoints + on Fuse F6 of power supply card PCB 43D
- on Fuse F5 if power supply card PCB 43D

The value should be between 12 and 15 VDC. The best is 13,5 V.

11.7. Test of 50 VAC :

Testpoints : on Fuse F5 on power supply card PCB 43D
on J26 pin on power supply card PCB 43D

The value should be between 45 to 55 VAC. The best is 52,5 V.

Note : the 50 VAC for the body of the bingo is tapped straightly from the transformer.

11.8. Test of G1 (6,3 VAC) :

Testpoint : J26, pins 10 and 14

Be careful : the G1 for the playfield is tapped straightly from the transformer.

11.9. Test of the battery voltage on computer card PCB 28 :

Testpoints + on Pin 22 from I.C. Q14
- on TP 6

Value : with voltage + 4,75, normal : 4.60 V
without voltage 3 to 4 V, normal 3,80 V

11.10. Test of the floating 12 V :

Between the floating 12 V and the 50 VAC 1 and 2, no direct connection may exist. In order to check this, one should disconnect the power supply and discharge the filter capacities by a short-circuit, straight or via a low resistor. The current shall have an extremely high value.

Successively one should measure between :

- Fuse F5 (VAC 1) on the power supply card PCB 43D
and
- Fuse F2 (power supply voltage for VCC), also on power supply card PCB 43

First check if there is OV between both cards :

- if not, cause a short-circuit again
- if yes, check whether there is a high resistance between both points. A value of 1M Ohm is still acceptable.

Repeat these manipulations between F5 and GND IC J26/1 or the negative of the filtercapacities.

CHAPTER 12 : PCB 28

PCB 28B = CPU = Central Processor Unit

12.1. 1 x 8085A = Microprocessor

8 bits

12.2 3 x 8155

ICs containing 3 distinctive sections

- 256 RAM bytes
- 3 programmable ports
- 1 programmable timer 14 bits

It is through the 3 x 3 ports of the 3 8155 that PCB 28B interrogates the switches and activates the motors and the lamps of the game.

To read the switches, these ports go through the optocouplers TIL 111 and to activate the relays of lamps and motors, they go through the Buffer Collectors open 7406.

12.3. 16 Optocouplers TIL 111

These are IC's with 6 pins, containing a LED which illuminates a PHOTOTRANSISITOR. When the LED ignites the phototransistor conducts.

12.4. 2 Memories RAM CMOS, type 5101

These are memories RAM 256 x 4 bits.

They are constantly kept under tension by 3 batteries 1,2V in serie = 3,6V.

When the machine is not connected, a tension of more than 3 up to 4 V DC has to be found on the Pins 22 of these 2 memories.

If this is not the case, verify the batteries, or the diode AAZ15 in serie with the batteries.

12.5. 6 Sockets 24 Pins destinated tp contain the programmed memories

These memories are initially EPROM's type 2716 INTEL = 2516 TEXAS. The PCB 28 B is already provided to receive EPROM's 2532 TEXAS or ROM's 2316 or 2332.

These memories EPROM 2516 are erasable by ultra-violet illumination.

12.6. Important

The program number of MISS AMERICANA TRIPLE BONUS is TBV 05.

There are 3 versions :

- TBV 05 : The number of steps required to lite the "BONUS"-boxes is variable
- TBV 05' : 16 steps are required to lite the "BONUS"-boxes
- TBV 05" : 32 steps are required to lite the "BONUS"-boxes

CHAPTER 13 : TROUBLE SHOOTING

It is just impossible to list all eventual defects in a technical manual. Anyway, the items mentioned below can be used as a basis for a fast analysis on defects.

13.1. Tilt lamp

In 'TILT', this lamp flashes, which means that the program is running. The microprocessor functions internally normal.

13.2. Stability of the 'DISPLAY' and the lamps on the frontpanel

The Replay Register should provide stable indications (should not flash) and the light of the lamps should be regular.

Every discrepancy (irregularity) means that the signals SCAN A, SCAN B, SCAN C, SCAN D are incorrect.

13.3. Errors in reading the switches

If the matrix of the switches states an irregular answer, check SCAN A, SCAN B, SCAN C, SCAN D. In order to locate the origin of the defect, disconnect successively :

J 10 (the display)
J 7 (the dipswitches)
J 5 (the switches from playfield and door)

Try to replace, just in an alternative way, IC 7475 and the 2 x 74145 and 7486 on Matrix PCB 32 ; finally computerboard PCB 28B.

13.4. Signals SCAN A/B/C/D

They serve at the same time for the interrogation of :

- the matrix of the play-contacts
- the matrix of the dipswitches of PCB 42
- lampmatrix of the frontpanel
- display 4 digits PCB 44

A defect in a certain matrix can influence other parts. Consequently : do not attach too much importance to a defect in reading one part. It occurs that all contacts are read erroneously by the microprocessor and that the repair of only one defect solves all problems.

Best way is to disconnect alternatively the different parts.

13.5. First : measure VCC 1 and VCC 2

Should be between 4,75 and 5,25 VDC.

13.6. Temperature of an IC

One can test easily with the back of his hand whether the temperature of an IC is too high, due to a short circuit. This applies especially to IC driver 7406 on PCB 28B.

13.7. If some lamps do not light up anymore or are too much enlightening.

Check whether they are put on same X-row or Y-column and replace the transistor driver from this X or Y (only when the replay register lights up in a stable way ; if not there is a defect in SCAN A/B/C)

13.8. Test and adjustment of PR1 or computercard PCB 28B

Put an oscilloscope on TP2 of computerboard PCB 28 and adjust PR1 to obtain a period of 2 to 2,2 milliseconds. The signal should be fully square waved.

A less accurate method is counting the number of flashings from the tiltlamp during 30 seconds : one should count approx. 100 flashes. In order to obtain them : adjust PR 1.

13.9. Test of SCAN A

Put an oscilloscope on pin 15 of IC Q5 (7445) on matrix-driver PCB 32. A square wave of 4 milliseconds should be observable.

13.10. Test of SCAN B

Put an oscilloscope on pin 14 OF IC Q5 (7445) on PCB 32. A square wave of 8 milliseconds should be observable.

13.11. Test of SCAN C

Put an oscilloscope on pin 13 of IC Q5 on matrixdriver PCB 32. A square wave of 16 milliseconds should be observable.

13.12. Test of the Reset Pulse

An oscilloscope on TP1 from computerboard PCB 28 states the reset if the level is low. If connecting the powerline, TP1 should remain low for approx. 0,2 seconds and then go up to 5 V; when disconnecting the powerline, TP1 should immediately go down.

Note : in order to obtain a reset from the microprocessor, one can connect TP1 without any danger for a short time to the mass.

13.13. Test of SCAN D

An oscilloscope on pin 12 of Q6 on the matrixdriver on PCB 32 should cause positive pulses during 2 milliseconds (no square wave)

CHAPTER 14 : LIST OF (ELECTRONIC) COMPONENTS

Principally, the indications correspond to those from the drawings.

<u>PARTNUMBERS</u>	<u>DESCRIPTION</u>
PCB 028	CENTRAL PROCESSOR UNIT
PCB 032	MATRIX DRIVER (MULTIPLEX)
PCB 033	BODY SPLIT
PCB 034	MAGIC MOTOR
PCB 035	INTERNAL TELEPHONEBOARD
PCB 036	TELEPHONEBOARD FOR TELEPHONEBOX
PCB 040	MAGIC LITES
PCB 042	DIPSWITCHES MATRIX
PCB 043	RECTIFIER
PCB 044	4 DIGITS DISPLAY
PCB 045	ELECTRONIC SOUND MODULE
PCB 046/1 THRU 5	BALL HOLE SWITCHES HOLDERS
PCB 067	SCORE LITES
PCB 072	SOUND COIL DRIVER
PCB 074	RANDOM NUMBER GENERATOR

In view of the considerable price of the memories, it is possible to obtain the computerboard without memories. This should be mentioned in case you order.

Even one memory only can be ordered, provided the bingomodel and the program-version are stated.

14.1. Electronical components inherent to the boards

A partnumber is composed with the aid of exploded view

e.g.

099/PCB 28-07 stands for PCB 28
103/PCB 032-07 stands for PCB 32
138/PCB 044-07 stands for PCB 44

For other ICs : consult notes R1/R2Q1C1 on the shematics and compose the number : e.g. component A4-PCB 28C-IC 8155

Note :

When ordering, one should always mention following details :

1. the name of the game : MISS AMERICANA TRIPLE BONUS
2. version of the program
3. the date

14.2. Flat cables

Resume the **LINK-number**, marked on the cables.
LK xx or xx = the link-number.

14.3. Cable-Form (harness of grouped wires)

Idem, the number H xx or xx is the number of the cable form.

14.4. The connectors

It is not recommendable at all to replace them, as they require special tools. Nevertheless, they are available.

Three types of connectors are used in the machines :

1st type : the connectors for flatcables of 16 - 34 - 50 wires.

2nd type : rectangular, white or brown nylon connectors type MAT'N LOCK (male or female pins can be obtained separately. Just quote the number of through connections and state the type : male or female)

3rd type : striped, red-brown nylon connectors, type MTA. Only used in a construction of ten contacts, for both male and female. In order to introduce the wires in those connectors one needs very expensive tools. For a little repair, one can solder the wire to the relative pin.

14.5. The motors

In case of an order, they require clear specification :

BALL LIFTER MOTOR : can be delivered as a separate unit or completely mounted. Please specify clearly when ordering.

14.6. The microswitches

Should be indicated by their abbreviation in CHAPTER X :
TEST OF THE ENTRIES, e.g. : DOOR SW, THROUGH SW,

CHAPTER 15 : LIST OF ADDRESSES ("SEEINSIDE")

15.1. The listing hereunder gives the most important symbolic addresses of the game and their value, as well as their function.

15.2. Steppers Score Red/Yellow/Green/White

<SCRSTP>	=	405C	<RPCNTR>	=	4060 - 1
<SCYSTP>	=	405D	<RPCNTY>	=	4062 - 3
<SCGSTP>	=	405E	<RPCNTG>	=	4064 - 5
<SCWSTP>	=	405F	<RPCNTW>	=	4066 - 7

15.3. Selection Feature Stepper

<SFSTP> = 405B

15.4. Extra Ball Stepper

<EBSTP> = 405A

15.5. Timer stepper

<TIMSTP> = 4059

15.6. Bonus Stepper

<BONSTP>	=	Yellow	=	4023
	=	Green	=	4024
	=	White	=	4025

15.7. Trip Relays

<TTILT>	=	4048	
<TSELB5>	=	4050	Select before 5
<TANY 2>	=	404B	
<TANY 3>	=	404C	
<T4STAR>	=	404D	Trip 4 Star as 5 in Line Green
<TOKMAK>	=	4068	
<TBEF4>	=	404A	Trip before 4st Ball
<TBEF5>	=	404F	Trip before 5th Ball
<TBONUS>	=	Yellow	= 4055
	=	Green	= 4056 Trip Bonus
	=	White	= 4057
<TBMAKE>	=	Yellow	= 402E
	=	Green	= 402F
	=	White	= 4030
<TCORN>	=	4052	Trip Corner

<TEB>	=	4049	Trip Extra Ball
<TEXCRD>	=	4051	Trip Extra Card
<TOK>	=	4069	Trip OK
<TROLLOV>	=	4053	Trip Rollover

15.8. Mixers Spot

<MIX1CNT>	=	4028	Mixer 1 Counter
<MIX2CNT>	=	4029	Mixer 2 Counter
<MIX3CNT>	=	402A	Mixer 3 Counter
<MIX4CNT>	=	402B	Mixer 4 Counter
<SPOCNT>	=	4027	Spotting Counter
<M4REL>	=	42BD	Mixer 4 Relays

15.9. Testgames

<POINT>	=	4034-5	Direct Indicator
<POINTX>	=	4036-7	Indirect Indicator

15.10. Reflex

<RFX>	=	4009	
-------	---	------	--

15.11. Hole Switch

<HOLESW1>	=	4137	= Sw N° 1
<HOLESW2>	=	4138	= Sw N° 2
<HOLESW3>	=	4139	= Sw N° 3
<HOLESW4>	=	413A	= Sw N° 4
<HOLESW5>	=	413B	= Sw N° 5
<HOLESW6>	=	413C	= Sw N° 6
<HOLESW7>	=	413D	= Sw N° 7
<HOLESW8>	=	413E	= Sw N° 8
<HOLESW9>	=	413F	= Sw N° 9
<HOLESW10>	=	4140	= Sw N° 10
<HOLESW11>	=	4141	= Sw N° 11
<HOLESW12>	=	4142	= Sw N° 12
<HOLESW13>	=	4143	= Sw N° 13
<HOLESW14>	=	4144	= Sw N° 14
<HOLESW15>	=	4145	= Sw N° 15
<HOLESW16>	=	4146	= Sw N° 16
<HOLESW17>	=	4147	= Sw N° 17
<HOLESW18>	=	4148	= Sw N° 18
<HOLESW19>	=	4149	= Sw N° 19
<HOLESW20>	=	414A	= Sw N° 20
<HOLESW21>	=	414B	= Sw N° 21
<HOLESW22>	=	414C	= Sw N° 22
<HOLESW23>	=	414D	= Sw N° 23
<HOLESW24>	=	414E	= Sw N° 24
<HOLESW25>	=	414F	= Sw N° 25

15.12. Internal Copies of the Totalising Counters

<TOTI>	=	400E / 400F / 4010	=	Total IN
<TOTO>	=	4011 / 4012 / 4013	=	Total OUT
<TELI>	=	4014 / 4015 / 1016	=	TEL IN
<TELO>	=	4017 / 4018 / 4019	=	TEL OUT
<CASH>	=	401A / 401B / 401C	=	Cashbox Meter

For all above-mentioned addresses, the first one is the lower significant byte.

15.13. Remote Control

<TELA>	=	4177
<TELB>	=	4178
<TEL C>	=	4179
<TELD>	=	417A
<TELOUT>	=	420F
<TELIN>	=	4210

15.14. Switches

<SHUSW>	=	4150	Shutter
<GATESW>	=	4151	Gate
<COSHU>	=	4152	Carry Over Shutter
<ROVRSW>	=	4153	Rollover Red
<ROVYSW>	=	4154	Rollover Yellow
<ALEYSW>	=	4155	Alley
<TRG1>	=	4157	Through 1
<TRG2>	=	4158	Through 2
<TRG3>	=	4159	Through 3
<TRG4>	=	415A	Through 4
<TRG7>	=	415B	Through 5
<COLIFT>	=	145C	Carry Over Lifter
<PULSLI>	=	415D	Pulse Ball Lifter
<MANLI>	=	415E	Manual Lift
<RBUT>	=	415F	R Button
<XBUT>	=	4160	X Button
<DOORSW>	=	4162	Door
<TRGO>	=	4163	Through 0
<TRG5>	=	4164	Through 5
<TRG6>	=	4165	Through 6
<TILTSW>	=	4167	Tilt
<REDBUT>	=	4168	Red Button
<YELBUT>	=	4169	Yellow Button
<ABUT>	=	416A	A Button
<BBUT>	=	416B	B Button
<CBUT>	=	416C	C Button
<DBUT>	=	416D	D Button
<EBUT>	=	416E	E Button
<STCY>	=	4298	Start Contact Game
<STLINA>	=	4246	Start Contact Magic Line A
<STLINB>	=	4247	Start Contact Magic Line B
<STLINC>	=	4248	Start Contact Magic Line C

<STLIND>	=	4249	Start Contact Magic Line D
<STLINE>	=	424A	Start Contact Magic Line E
<MOTLIF>	=	4219	Ball Lifter Motor
<MOTSHU>	=	421A	Shutter Motor
<MOTA>	=	4213	Magic Motor A
<MOTB>	=	4214	Magic Motor B
<MOTC>	=	4215	Magic Motor C
<MOTD>	=	4216	Magic Motor D
<MOTE>	=	4217	Magic Motor E

15.15.SB1

<SV1>	=	4171
<SV2>	=	4172
<SV3>	=	4173
<SV4>	=	4174
<SV5>	=	4175
<SV6>	=	4176

15.16.Special Locations

<M4REL>	=	42BD	Bonus Yellow
<DIMINT>	=	4319	Bonus Green White
<BCNT>	=	431F	Bonus Counter
<DIPSW>	=	4076	Dipswitches Group D
	=	4077	Dipswitches Group C
	=	4078	Dipswitches Group B
	=	4079	Dipswitches Group A
	=	407A	Dipswitches Group E
	=	407B	Dipswitches Group F
	=	407C	Dipswitches Group G
	=	407D	Dipswitches Group H
<MLAST>	=	424B	Sw Magic Motor A Status
	=	424C	Sw Magic Motor B Status
	=	424D	Sw Magic Motor C Status
	=	424E	Sw Magic Motor D Status
	=	424F	Sw Magic Motor E Status
<GAME>	=	4294	Location on FF if "Game Status"
<COIN1>	=	416F	Coin Switch N° 1
<COIN2>	=	4170	Coin Switch N° 2
<LSREL>	=	4245	Lifter Start Relay
<RPREG>	=	4007-8	Replay Register
<RPREGB>	=	4004-5	Replay Register Copy
<GT9>	=	4020	Testify. If = 4022 : Error

15.17. Hexadecimal Codes

REPRESEN-TATION -	HEXADECI-MAL CODE-	BIT 3	BIT 2	BIT 1	BIT 0	DECIMAL CODE
		D (8)	C (4)	B (2)	A (1)	
□	0	0	0	0	0	0
	1	0	0	0	I	1
2	2	0	0	I	0	2
3	3	0	0	I	I	3
4	4	0	I	0	0	4
5	5	0	I	0	I	5
6	6	0	I	I	0	6
7	7	0	I	I	I	7
8	8	I	0	0	0	8
9	9	I	0	0	I	9
A	A	I	0	I	0	10
B	B	I	0	I	I	11
C	C	I	I	0	0	12
D	D	I	I	0	I	13
E	E	I	I	I	0	14
OFF	F	I	I	I	I	15

15.18. Service Box SB1

- Switch SV1 :

an address will be displayed (4009 if machine is switched on). With switches SV2 (+ 1) and SV3 (- 1) the address can be increased or decreased. The display represents hexadecimal code (7 segments)./
- Switch SV4 (SEEBUT) :

The contents of the address that has been selected will be displayed on the two right figures. The two left figures flash : they represent the contents of the following address.
- By keeping SV4 switched on, SV2 and SV3 will allow you to get +1 or -1 to the contents of the selected address.

Note that $00 - 1 = FF$
 $FF + 1 = 00$
- Service Box SB1 will thus allow you to choose a position on any address whatsoever, to read it and eventually to change its contents.

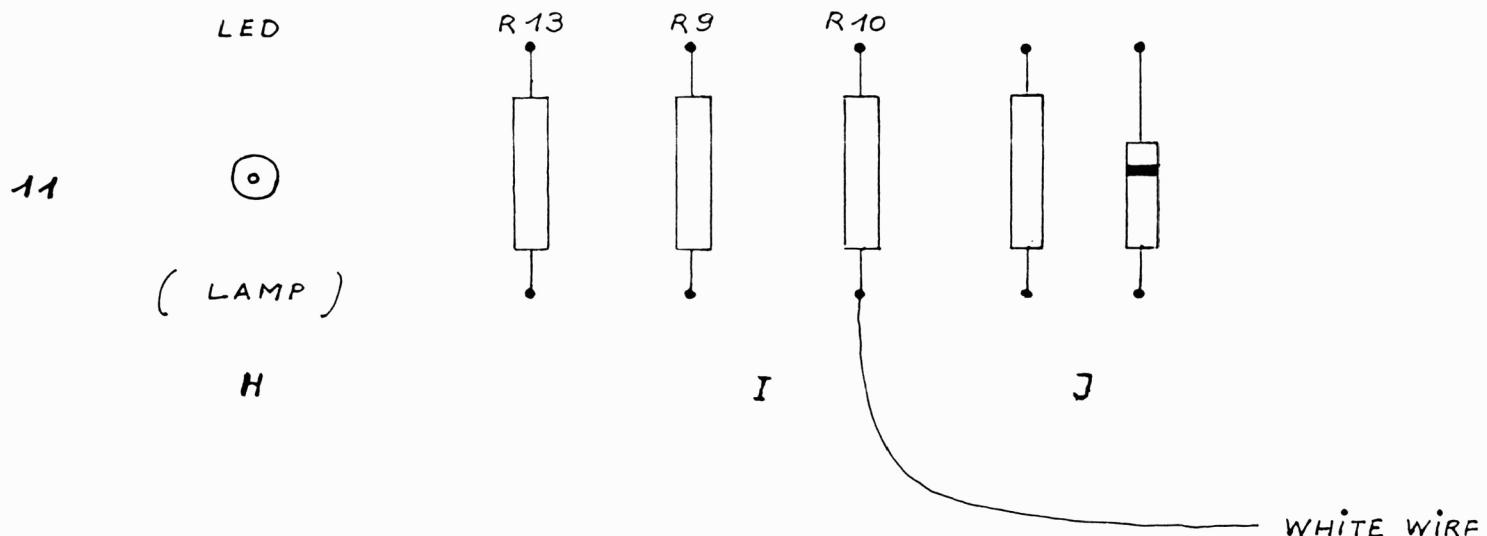
CHAPTER 16 : CONNECTION AND ADJUSTMENT
OF ANTICHEAT (PCB 100)

This board safeguards the bingo against piezo electricity.

Connections :

The bipolar plugs with brown and black wires provide the card with current and should be enclosed between the matrixdriver PCB 32 plug J 14 and the computerboard PCB 28 plug J 14.

The white wire must be connected on the computerboard PCB 28 between R9 and R10 :



The 6-polar connector must be connected to the anticheat card PCB 100.

The red wire is the antenna that will capture spikes and will put the computer out of order.

Adjustment :

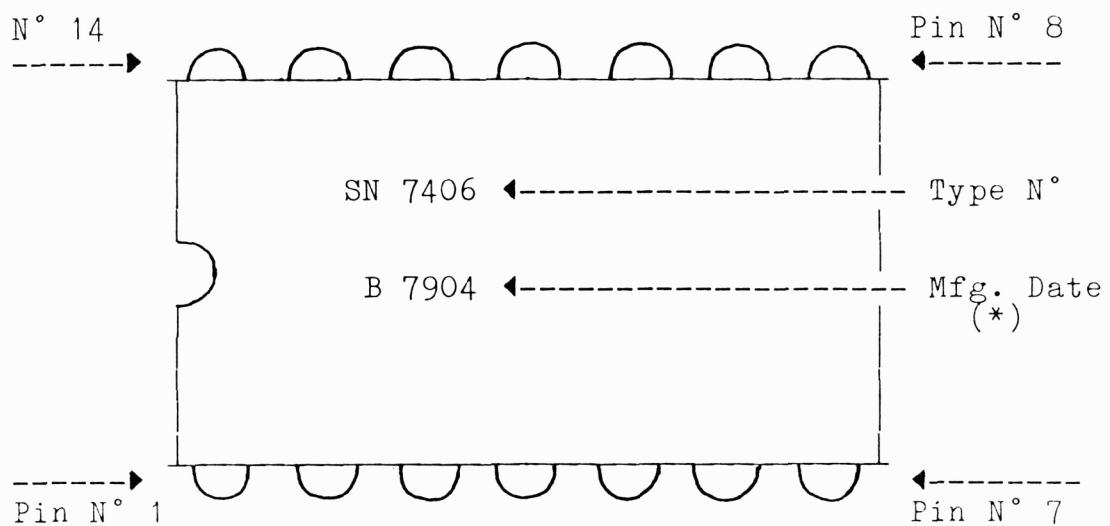
By turning the potentiometer on the anticheatboard, one can adjust the sensitivity of the antenna. By turning clockwise one obtains a decrease of the sensitivity. If the sensibility remains too high, one can shorten the antenna, taking into account that the antenna should always be longer than 50 cm.

It is impossible to adjust the sensitivity at the factory in such a way that it complies in every location, as the quality of the electrical installation and the kind of electrical equipment in the neighbourhood of the bingo are of too much importance. The last adjustment should be done on the spot.

CHAPTER 17 : INTEGRATED CIRCUITS

17.1. Location of Pin Nbr. 1 of an I.C.

TOP VIEW OF A COMPONENT



(*) 4th week of the year 1979

17.2. The Power Supply Pins

The power supply :

- in VCC = + 5V goes through Pin 14 (IC 14 Pins) or Pin 16 (IC 16 Pins)
- in GND = GROUND = -5V goes through Pin 7 (IC 14 Pins) or Pin 8 (IC 16 Pins)

Data Sheet : 8085
 8155
 5101
 2716
 8212
 7400
 7402
 7406-7416
 7417
 7445/145
 7474
 8205(74 LS 138)
 7414



8085A/8085A-2 SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3 μ s Instruction Cycle (8085A);
0.8 μ s (8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64k Bytes of Memory

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

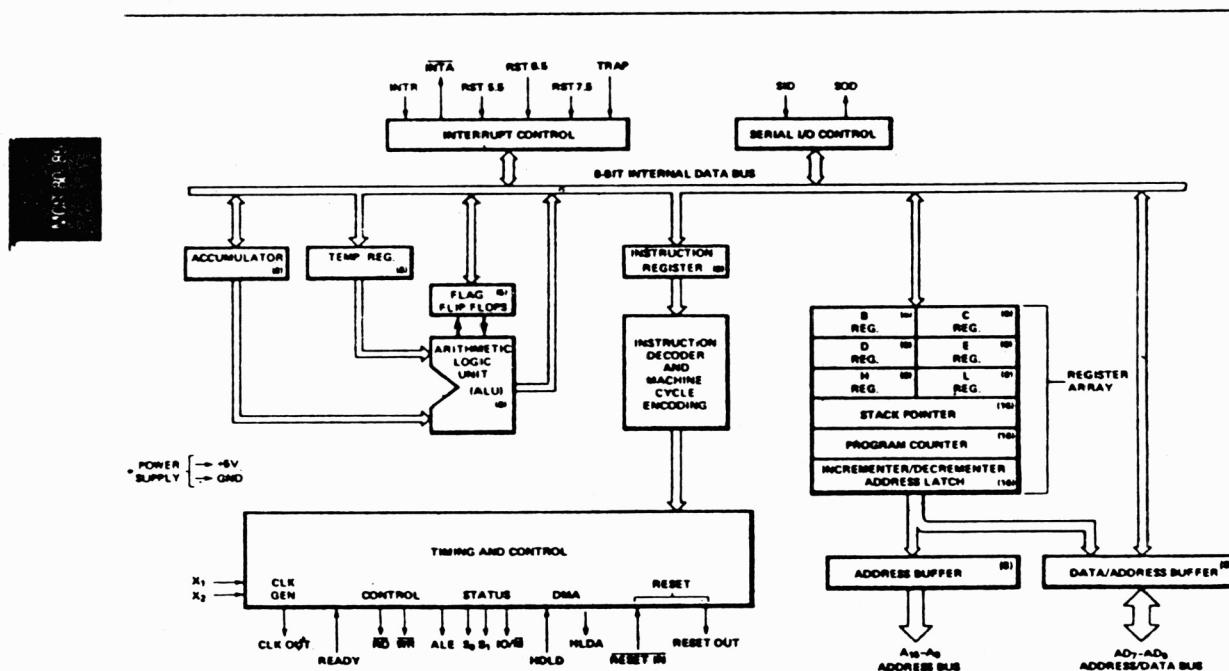


Figure 1. 8085A CPU Functional Block Diagram

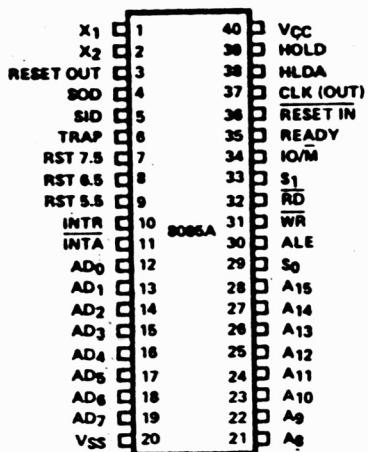
8085A/8085A-2

Figure 2, 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

<u>Symbol</u>	<u>Function</u>																																								
A8-A15 (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address. 3-stated during Hold and Halt modes and during RESET.																																								
AD0-7 (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.																																								
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.																																								
S0, S1, and IO/M (Output)	Machine cycle status: <table border="1"> <thead> <tr> <th>IO/M</th> <th>S1</th> <th>S0</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Memory write</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Memory read</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>I/O write</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>I/O read</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Opcode fetch</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Interrupt Acknowledge</td> </tr> <tr> <td>*</td> <td>0</td> <td>0</td> <td>Halt</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Hold</td> </tr> <tr> <td>*</td> <td>X</td> <td>X</td> <td>Reset</td> </tr> </tbody> </table> <p>* = 3-state (high impedance) X = unspecified</p>	IO/M	S1	S0	Status	0	0	1	Memory write	0	1	0	Memory read	1	0	1	I/O write	1	1	0	I/O read	0	1	1	Opcode fetch	1	1	1	Interrupt Acknowledge	*	0	0	Halt	*	X	X	Hold	*	X	X	Reset
IO/M	S1	S0	Status																																						
0	0	1	Memory write																																						
0	1	0	Memory read																																						
1	0	1	I/O write																																						
1	1	0	I/O read																																						
0	1	1	Opcode fetch																																						
1	1	1	Interrupt Acknowledge																																						
*	0	0	Halt																																						
*	X	X	Hold																																						
*	X	X	Reset																																						
RD (Output, 3-state)	READ control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. 3-stated during Hold and Halt modes and during RESET.																																								
WR (Output, 3-state)	WRITE control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.																																								
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.																																								
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated.																																								
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.																																								
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTRO is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.																																								



8085A/8085A-2

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
<u>INTA</u> (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.		Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as RESET IN is applied.
<u>RST 5.5</u> <u>RST 6.5</u> <u>RST 7.5</u> (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.	<u>RESET OUT</u> (Output)	Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
<u>TRAP</u> (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)	<u>X₁, X₂</u> (Input)	X ₁ and X ₂ are connected to a crystal, LC, or RC network to drive the internal clock generator. X ₁ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
<u>RESET IN</u> (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a	<u>CLK</u> (Output)	Clock Output for use as a system clock. The period of CLK is twice the X ₁ , X ₂ input period.
		<u>SID</u> (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
		<u>SOD</u> (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
		<u>Vcc</u>	+5 volt supply.
		<u>Vss</u>	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

- (1) The processor pushes the PC on the stack before branching to the indicated address.
- (2) The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.



8155/8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

8155 — Active Low Chip Enable (\overline{CE})
8156 — Active High Chip Enable (CE)

*Directly Compatible with 8085A CPU

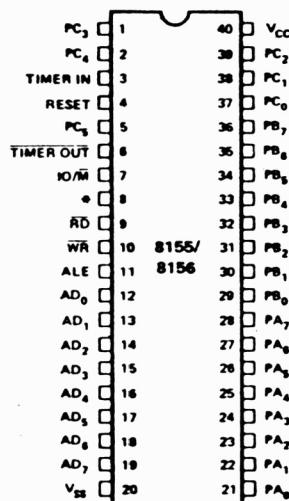
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6 Bit I/O Port
- Programmable 14 Bit Binary Counter/Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in 8085A CPU.

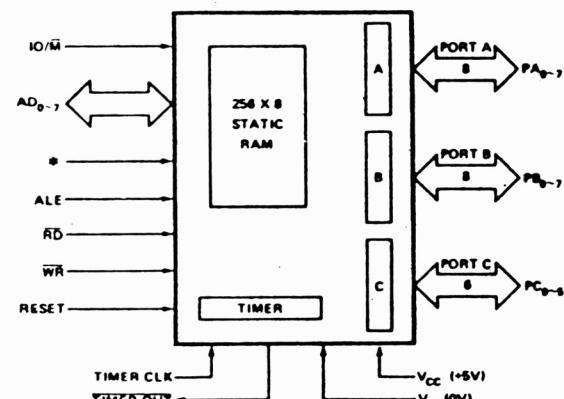
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14 bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



* : 8155 = \overline{CE} , 8156 = CE

8155/8156

8155/8156 FUNCTIONAL PIN DEFINITION

The following describes the functions of all of the 8155/8156 pins.

<u>Symbol</u>	<u>Function</u>	<u>Symbol</u>	<u>Function</u>
RESET	The Reset signal is a pulse provided by the 8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be 600 nsec. (Two 8085A clock cycle times).	PA ₀₋₇ (8)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
AD ₀₋₇	These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/M input signal. The 8-bit data is either written into the chip or Read from the chip depending on the status of WRITE or READ input signal.	PB ₀₋₇ (8)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.
CE or \overline{CE}	Chip Enable: On the 8155, this pin is CE and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.	PC ₀₋₅ (6)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When PC ₀₋₅ are used as control signals, they will provide the following: PC ₀ — A INTR (Port A Interrupt) PC ₁ — A BF (Port A Buffer full) PC ₂ — $\overline{A STB}$ (Port A Strobe) PC ₃ — B INTR (Port B Interrupt) PC ₄ — B BF (Port B Buffer Full) PC ₅ — B STB (Port B Strobe)
RD	Input low on this line with the Chip Enable active enables the AD ₀₋₇ buffers. If IO/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.	TIMER IN	This is the input to the counter timer.
WR	Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of IO/M.	TIMER OUT	This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.
ALE	Address Latch Enable: This control signal latches both the address on the AD ₀₋₇ lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.	V _{CC}	+5 volt supply.
IO/M	IO/Memory Select: This line selects the memory if low and selects the IO if high.	V _{SS}	Ground Reference.



2716 16K (2Kx8) UV ERASABLE PROM

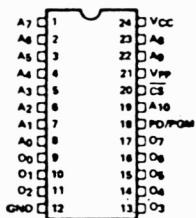
- Single +5V Power Supply
- Simple Programming Requirements
Single Location Programming
Programs With One 50ms Pulse
- Low Power Dissipation
525mW Max. Active Power
132mW Max. Standby Power
- Pin Compatible To Intel 2316E ROM
- Fast Access Time: 450ns Max.
- Inputs and Outputs TTL
Compatible During Read
And Program

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static power down mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical. For production quantities, the 2716 user can convert rapidly to Intel's new pin-for-pin compatible 16K ROM, the 2316E.

Since the 450-nsec 2716 operates from a single 5-volt supply, it is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8048. The 2716 is also the first EPROM with a static power down mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now, it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



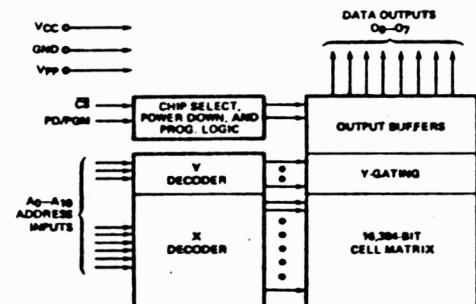
PIN NAMES

A ₀ -A ₁₀	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
CS	CHIP SELECT
O ₀ -O ₇	OUTPUTS

MODE SELECTION

PINS MODE	PD/PGM (18)	CS (20)	V _{PP} (21)	V _{CC} (24)	OUTPUTS (8-11, 13-17)
Read	V _{IL}	V _{IL}	+5	+5	D _{OUT}
Don't Care	Don't Care	V _{IL}	+5	+5	High Z
Power Down	V _{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V _{IL} to V _{IH}	V _{IL}	+25	+5	D _{IN}
Program Verify	V _{IL}	V _{IL}	+25	+5	D _{OUT}
Program Inhibit	V _{IL}	V _{IL}	+25	+5	High Z

BLOCK DIAGRAM





8212 = 745412

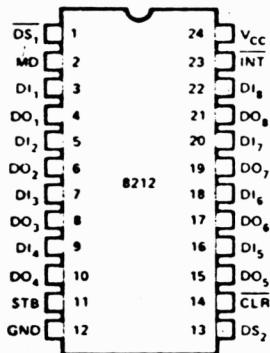
EIGHT-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

PIN CONFIGURATION

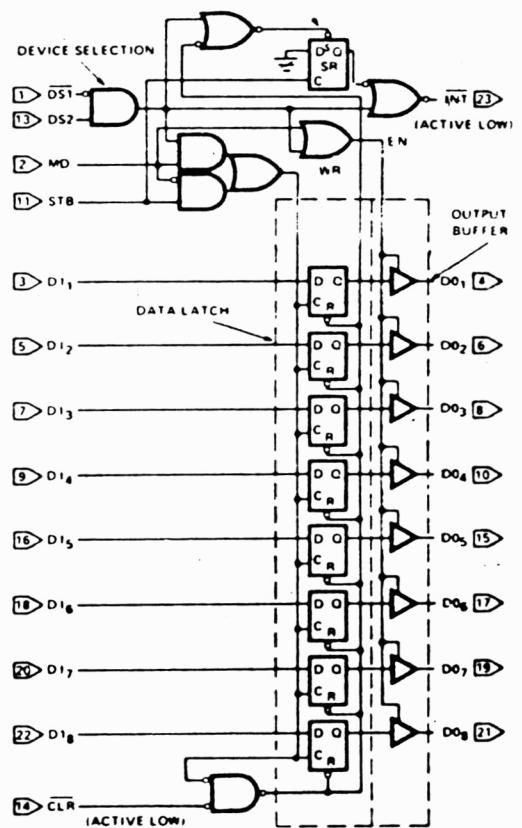


PIN NAMES

DI ₁ -DI ₈	DATA IN
DO ₁ -DO ₈	DATA OUT
DS ₁ , DS ₂	DEVICE SELECT
MD	MODE
STB	STROBE
INT	INTERRUPT (ACTIVE LOW)
CLR	CLEAR (ACTIVE LOW)

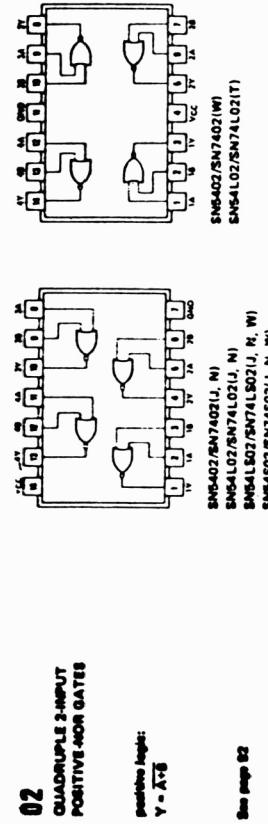
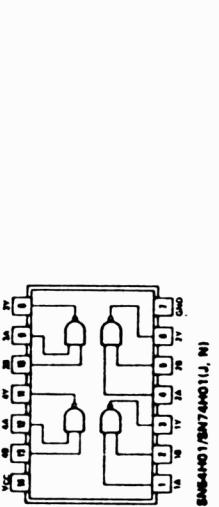
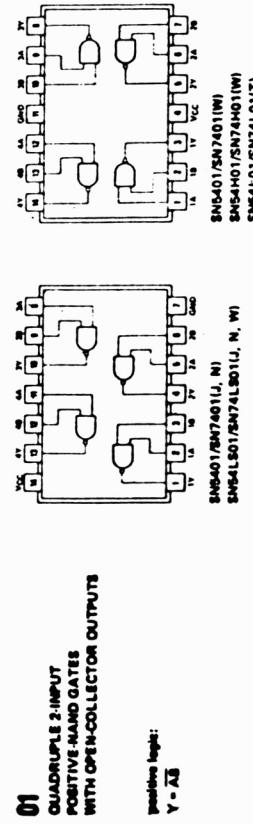
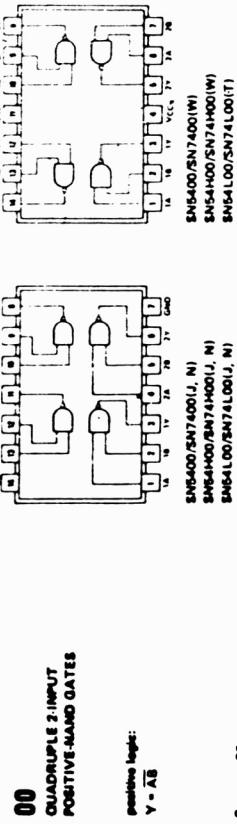
LOGIC DIAGRAM

SERVICE REQUEST FF

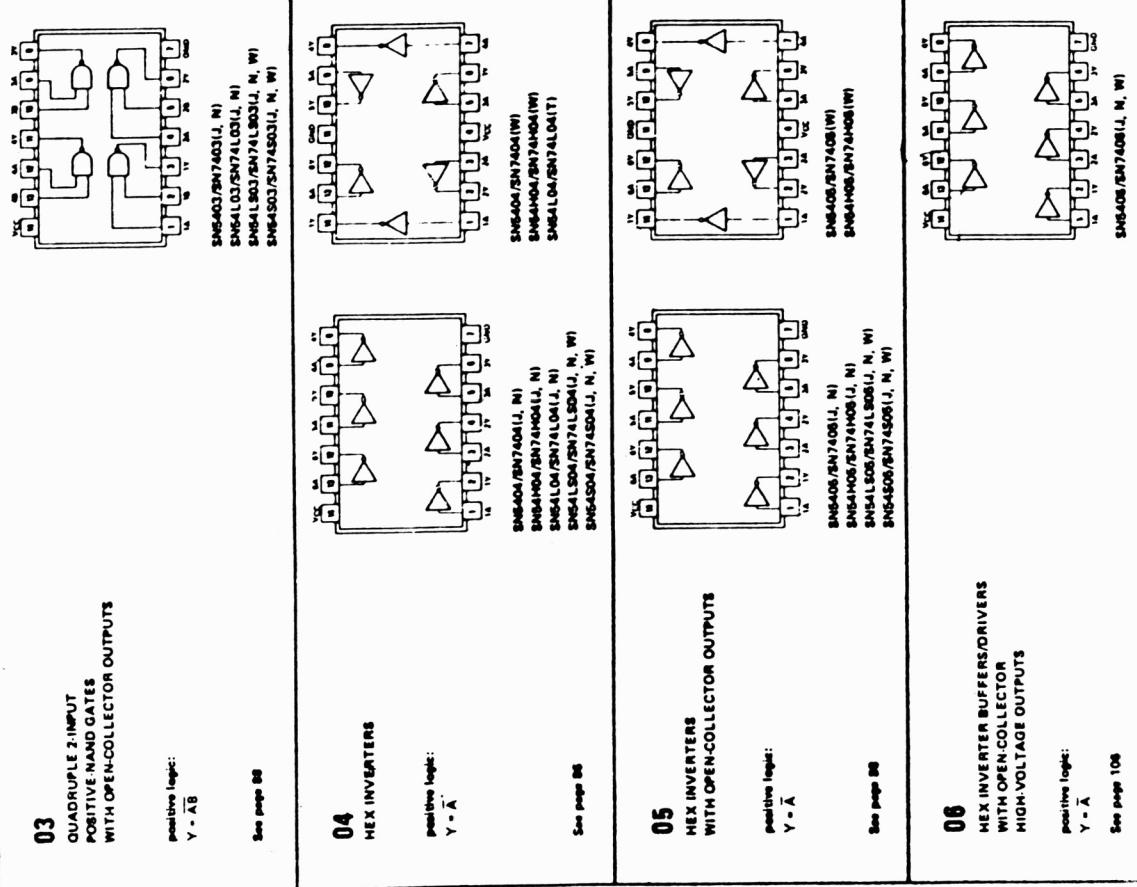


54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES...LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)



SSI GATES...LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)



TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

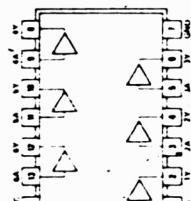
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

07
HEX BUFFER/INVERTERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:

$V = A$

See page 98



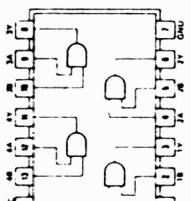
SN5407/SN7407(J, N, W)

08
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:

$V = AB$

See page 98



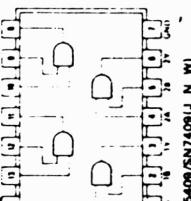
SN5408/SN7408(J, N, W)

09
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$V = AB$

See page 98



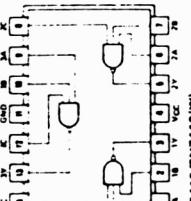
SN5409/SN7409(J, N, W)

10
TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:

$V = \bar{A}$

See page 98



SN5410/SN7410(J, N, W)

11
TRIPLE 3-INPUT
POSITIVE-AND GATES

positive logic:

$V = ABC$

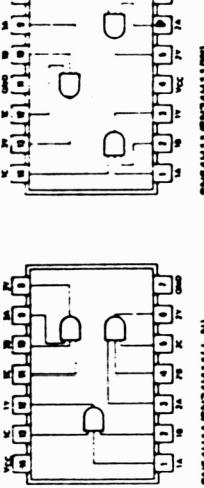
See page 98

11
TRIPLE 3-INPUT
POSITIVE-AND GATES

positive logic:

$V = ABC$

See page 98



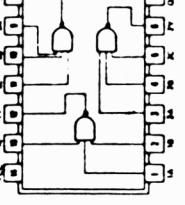
SN5411/SN7411(W)

12
TRIPLE 3-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$V = \bar{ABC}$

See page 98



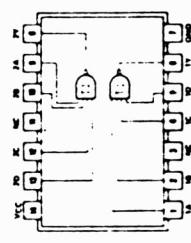
SN5412/SN7412(J, N, W)

13
DUAL 4-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

positive logic:

$V = ABCD$

See page 98



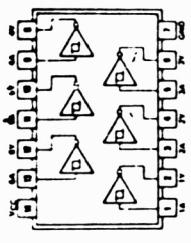
SN5413/SN7413(J, N, W)

14
HEX SCHMITT-TRIGGER
INVERTERS

positive logic:

$V = \bar{A}$

See page 98



SN5414/SN7414(J, N, W)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

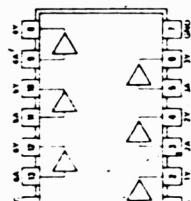
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

07
HEX BUFFER/INVERTERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:

$V = A$

See page 98



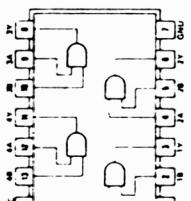
SN5407/SN7407(J, N, W)

08
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:

$V = AB$

See page 98



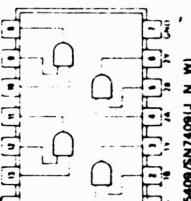
SN5408/SN7408(J, N, W)

09
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$V = AB$

See page 98



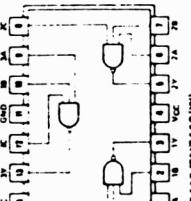
SN5409/SN7409(J, N, W)

10
TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:

$V = \bar{A}$

See page 98



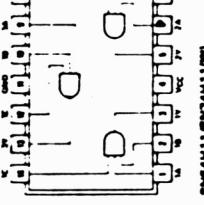
SN5410/SN7410(J, N, W)

11
TRIPLE 3-INPUT
POSITIVE-AND GATES

positive logic:

$V = ABC$

See page 98



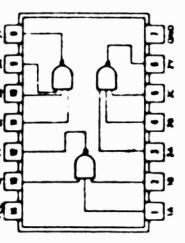
SN5411/SN7411(W)

12
TRIPLE 3-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$V = \bar{ABC}$

See page 98



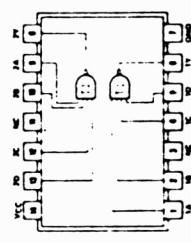
SN5412/SN7412(J, N, W)

13
DUAL 4-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

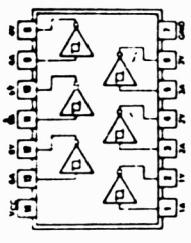
positive logic:

$V = ABCD$

See page 98



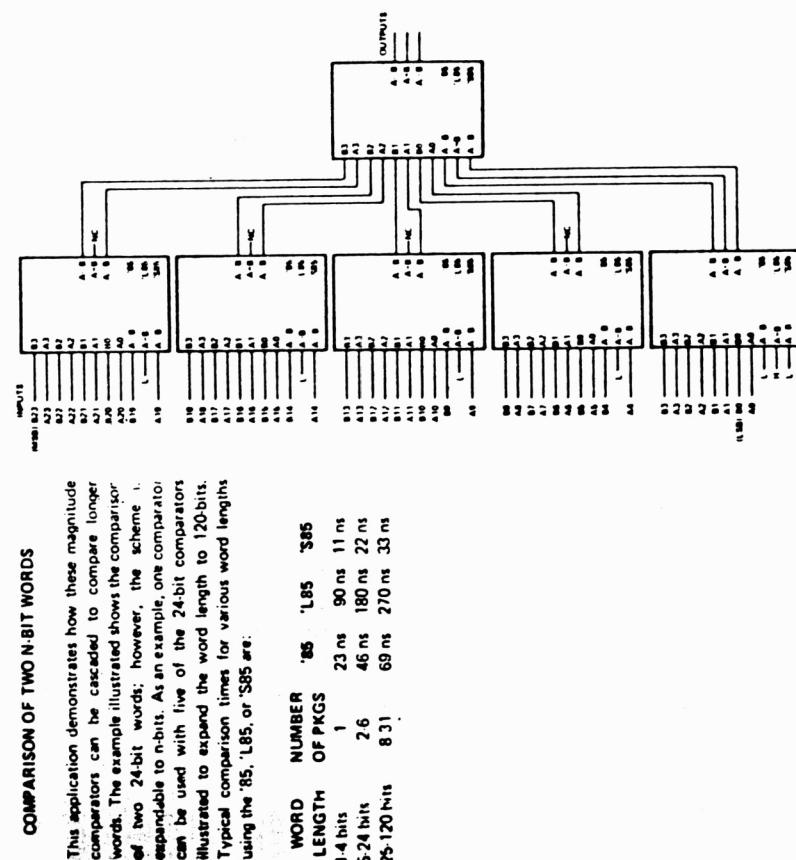
SN5413/SN7413(J, N, W)



SN5414/SN7414(J, N, W)

**TYPES SN54485, SN54L85, SN54S85,
485, SN74L85, SN74S85
T MAGNITUDE COMPARATORS**

TYPICAL APPLICATION DATA



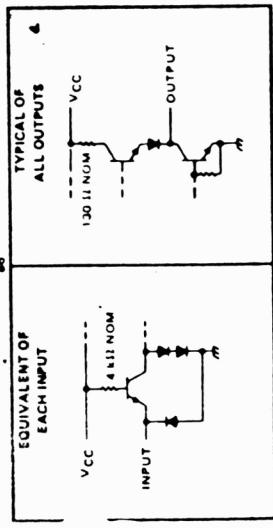
COMPARISON OF TWO 24-BIT WORDS

**TYPES SN54L86, SN54LS86, SN54S86,
SN74L86, SN74LS86, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

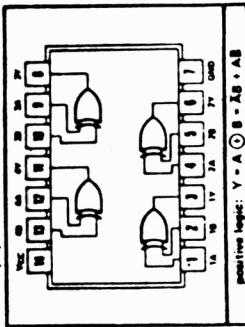
BULLETIN NO. DL-8 7/21/62, DECEMBER 1972

SCHEMATICS OF INPUTS AND OUTPUTS

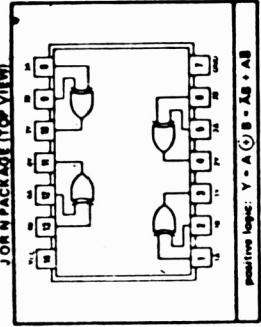
'LS86



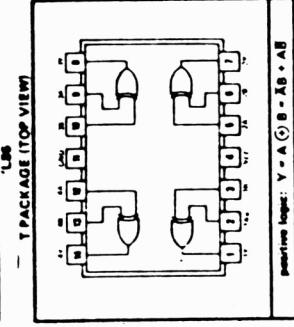
'L86, '74L86



'J86



'T86



FUNCTION TABLE

INPUTS	OUTPUT
A = L	Y = L
B = L	Y = L
A = H	Y = H
B = H	Y = H
A = H	Y = L
B = L	Y = H

H = High level, L = Low level

TYPE	TYPICAL PROPAGATION DELAY TIME	TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

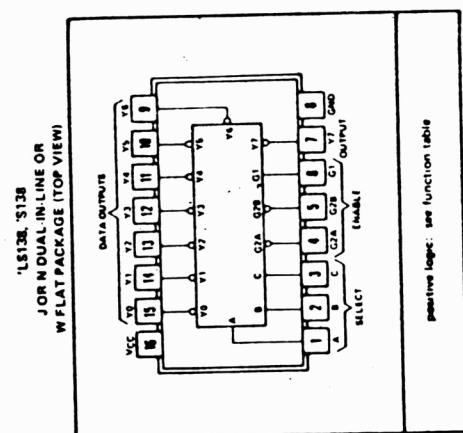
TYPES SN54LS138, SN54LS139, SN74LS138, SN54S139,
TTL SN74LS139, SN74LS138, SN74S138, SN74S139
MSI DECODERS/DEMULTIPLEXERS

BUREAU OF THE BUDGET
BUDGET NO. D-1 \$1211804, DECEMBER 1972

- Designed Specifically for High-Speed Memory Decoders
 - Data Transmission Systems
 - '5138 and 'LS138 3-to-8-Line Decodes Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
 - '5139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/Demultiplexers
 - Schottky Clamped for High Performance

TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION	
		22 nsec	32 mW
LS130	22 nsec	246 mW	34 mW
LS131	8 nsec	246 mW	300 mW
LS132	22 nsec	7.5 mW	7.5 mW
LS133	7.5 nsec	7.5 mW	7.5 mW

dition



These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory decoding or data-routing applications requiring very short propagation delay times. In high performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

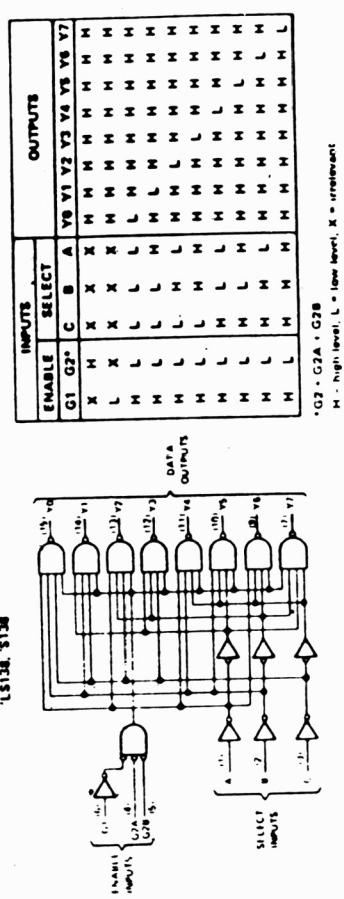
The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS130 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74S load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ring-ing and simplify system design. Series 54LS and 74S devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 741S and 741D devices are characterized for 0°C to 70°C industrial systems.

TYPES SN54LS138, SN54S138, SN54LS139, SN54S139
SN74LS138, SN74S138, SN74LS139, SN74S139
DECODERS/DEMULTIPLEXERS

Functional block diagrams and logic



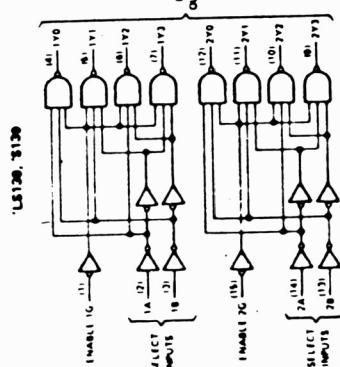
PUNCTUATION MARKS

G2 + G2A + G2B
H = high level, L = low level, X = irrelevant

LEACH DECODE AND DEMUX (PLEXER)
L3120, B130

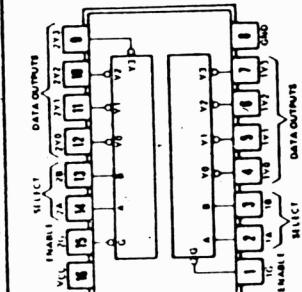
INPUTS		OUTPUTS			
ENABLE	SELECT	Y0	V1	V2	V3
		0	A	B	C
0	0	X	L	L	X
0	1	X	L	L	X
1	0	L	L	X	X
1	1	L	L	X	X

卷之三



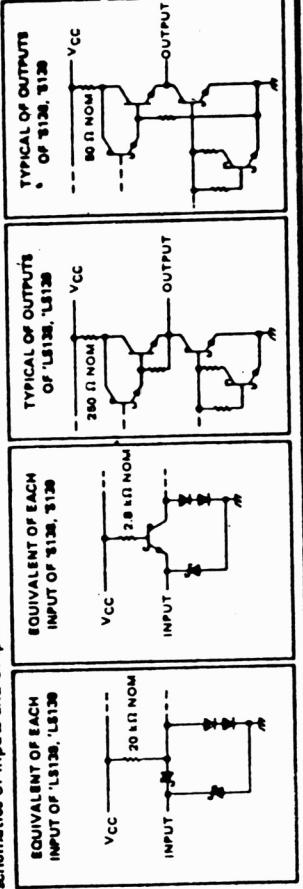
۲۱۳

JORN DUAL-IN-LINE OR
FLAT PACKAGE (TOP VIEW)



卷之三

EQUIVALENT OF EACH
INPUT OF \$125. REVENUE



TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

SN5445, SN7445 0-DECIMAL DECODERS/DRIVERS

TYPE: SN5446A, SN5447A, SN5448, SN5449, SN5440, SN5446, SN7446A, SN7447A, SN7448, SN7449, SN7446, SN7447
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

maximum ratings over operating free air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (or V _{IN}) at all operating temperatures	5.5 V
Maximum current into any output (off state)	1 mA
Operating temperature range, SN5445 Circuits	-55°C to 125°C
Operating temperature range, SN7445 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	SN5445			SN7445		
		MIN	NOM	MAX	MIN	NOM	MAX
High input voltage	V _{IL} = 0.8 V	7	7	V	0.8	0.8	V
Low input voltage	V _{IL} = 0.8 V	1.1	1.1	V	1.1	1.1	V
Output saturation voltage	V _{OL} = 0.8 V	12 mA	12 mA	1	80 mA	80 mA	1
Output saturation current	V _{OL} = 0.8 V	V _{IL}	V _{IL}	V _{IL}	V _{OL}	V _{OL}	V _{OL}
Output saturation voltage	V _{OL} = 0.8 V	10	10	V	0.5	0.5	V
Output saturation current	V _{OL} = 0.8 V	20 mA	20 mA	1	0.4	0.4	1
Signal-to-noise ratio at output voltage	V _{OL} = 0.8 V	10	10	V	1	1	V
High input current	V _{IL} = 0.8 V	40	40	1	2 A	2 A	1
Input current (off state)	V _{IL} = 0.8 V	1.6	1.6	1.6	1.6	1.6	1.6
Output current	V _{OL} = 0.8 V	4.3	4.3	6.2	4.3	4.3	7
Output current	V _{OL} = 0.8 V	4.3	4.3	7	4.3	4.3	7

Notes: 1. All ratings are guaranteed by test. 2. All ratings are guaranteed by design.

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5446A			SN7446A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5447A			SN7447A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5448A			SN7448A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5449A			SN7449A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5440A			SN7440A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5446			SN7446			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5447			SN7447			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5448			SN7448			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5449			SN7449			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5440			SN7440			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5446A			SN7446A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5447A			SN7447A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5448A			SN7448A			
		MIN	TYP	MAX	UNIT	MIN	TYP	MAX
Propagation delay, low to high, input signal	t _{LH} = 15 ns, t _{HL} = 100 ns, t _{PHL} = 100 ns	50	ns	50	ns	50	ns	50
Conduction delay, low to high, output signal								

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN5449A			SN7449A		

'S SN5446A, SN5447A, SN5448, SN5449, SN5446, SN5447,
SN7446A, SN7447A, SN7448, SN7449, SN7446, SN7447
TEN-SEGMENT DECODERS/DRIVERS.

TYPES SN5446A, SN5447A, SN5448, SN5449, SN5446, SN5447A, SN7446A, SN7447A, SN7448, SN7449, SN7446, SN7447A
BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS

option (continued)

The '46A, '47A, '48, '49, and 'L47 circuits incorporate automatic leading and/or trailing-edge zero-blanking control for RBO and RBO. Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. Lamp test (LT) of these types contain an overriding blanking input (BI1) which can be used to control the lamp intensity by pushing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 84 and Series 84L devices are characterized for operation over the full military temperature range of -55°C to +125°C; Series 74 and Series 74L devices are characterized for operation from 0°C to 70°C.

A vertical stack of ten rectangular boxes, arranged in two columns of five. The boxes contain the following symbols from top to bottom:
1. A small square with a diagonal line.
2. A small circle with a dot in the center.
3. A small square with a cross inside.
4. A small circle with a horizontal line through it.
5. A small square with a vertical line through it.
6. A small circle with a diagonal line.
7. A small square with a horizontal line.
8. A small circle with a vertical line.
9. A small square with a dot in the center.
10. A small circle with a dot in the center.

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FUNCTION TABLE -

DECIMAL OR FUNCTION	INPUTS				SI/RBO ¹	OUTPUTS				NOTE
	LT	RBI	D	C		■	■	■	■	
0	H	H	L	L	L	H	ON	ON	ON	OFF
1	H	X	L	L	L	X	OFF	ON	OFF	OFF
2	X	X	L	L	L	X	ON	OFF	ON	ON
3	X	X	X	L	L	X	ON	ON	OFF	OFF
4	X	X	X	X	L	X	OFF	ON	ON	ON
5	X	X	X	X	X	X	ON	ON	ON	ON
6	X	X	X	X	X	X	OFF	ON	ON	ON
7	X	X	X	X	X	X	ON	ON	ON	OFF
8	X	X	X	X	X	X	ON	ON	OFF	ON
9	X	X	X	X	X	X	OFF	ON	ON	ON
10	X	X	X	X	X	X	ON	OFF	ON	ON
11	X	X	X	X	X	X	OFF	ON	OFF	ON
12	X	X	X	X	X	X	OFF	ON	OFF	OFF
13	X	X	X	X	X	X	ON	OFF	ON	ON
14	X	X	X	X	X	X	OFF	OFF	ON	ON
15	X	X	X	X	X	X	OFF	OFF	OFF	OFF
16	X	X	X	X	X	X	L	L	X	X

In level 1, code levels, X = intermediate

1. The blanking input (B1) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (B1), all segment outputs are off regardless of the level of any other input.
3. When ripple blanking inputs (R11) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (R10) goes to a low level (resistor condition).
4. When the blanking input/ripple blanking output (B1/R10) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

AND logic requirement: In blanking input (B1) and/or ripple blanking output (R10),

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS				B1/RBO ¹	OUTPUTS	NOTE
	LT	RBI	D	C			
0	-	-	-	-	-	-	-
1	-	-	-	-	-	-	-
2	-	-	-	-	-	-	-
3	-	-	-	-	-	-	-
4	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-
6	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-
10	-	-	-	-	-	-	-
11	-	-	-	-	-	-	-
12	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-
14	-	-	-	-	-	-	-
15	-	-	-	-	-	-	-
					B1	RBI	LT

H = HIGH level L = LOW level X = INHIGH

NOTES - 1 The blanking input (B1) must be open or held at a high logic level when output functions C through G are desired. The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

2 When a low logic level is applied directly to the blanking input (B1), all segment outputs are low regardless of the level of any other input.

3 When ripple blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp go input and the ripple blanking output (RBO) goes to a low level (redzone condition), both the blanking input and the ripple blanking output (B1-RBO) is open or held high and a low is applied to the lamp segment outputs are high.

4 When the blanking input is open or ripple blanking output (B1-RBO) is open or held high, all segment outputs are high.

1

FUNCTION TABLE		NOTE																
OUTPUTS																		
FUNCTION	INPUTS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
		1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		2	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
		3	2	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13
		4	3	2	1	0	1	2	3	4	5	6	7	8	9	10	11	12
		5	4	3	2	1	0	1	2	3	4	5	6	7	8	9	10	11
		6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	9	10
		7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	9
		8	7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8

NOTES: 1. The digital input X must be open or held at a high logic level when output functions Q through 15 are desired.
2. When one logic level is applied directly to the binning input (B1), all segment outputs are now regardless of the level of any

TYPES SN54L42, SN54L43, SN54L44, SN74L42, SN74L43, SN74L44

BCD-TO-10-LINE DECODERS (10F-10)

TYPES SN5445, SN7445 BCD-TO-DECIMAL DECODERS/DRIVERS

REPLACES NO. DS-7213B, DEC 1972

maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54L42	SN74L42	SN54L43	SN74L43	SN54L44	SN74L44	UNIT
MIN	5	5	4.75	5	5.25	V	NOM
MAX	5.5	5.5	5	5	5.25	V	NOM
V _{CC} , input, V _{CC}	-400	-400	-400	-400	-400	mA	
Output current, I _{OH}	8	8	8	8	8	mA	
Output current, I _{OL}	55	125	0	70	70	mA	
Free air temperature, T _A							°C

maximum ratings over operating free-air temperature range (unless otherwise noted)

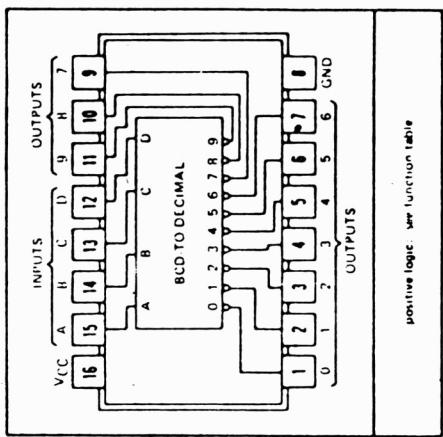
	TEST CONDITIONS ¹	MIN	TYP.	MAX	UNIT
		2	V	7	V
High-level input voltage	V _{CC} - MIN, I _I = 12 mA	0.8	V	1.5	V
One-level input voltage	V _{CC} - MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = 400 μ A	2.4	V	3.4	V
High-level output voltage	V _{CC} - MIN, V _{OH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 400 μ A	0.7	V	0.4	V
One-level output voltage	V _{CC} - MIN, V _{OH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 400 μ A	1	mA	1	mA
Input current at maximum input voltage	V _{CC} - MAX, V _I = 5.5 V	20	mA	20	mA
High-level input current	V _{CC} - MAX, V _I = 4 V	0.8	mA	0.8	mA
One-level input current	V _{CC} - MAX, V _I = 0.4 V	9	mA	20	mA
Short-circuit output current ²	V _{CC} - MAX, V _I = 0.4 V	14	mA	27	mA
Supply Current	See Note 2	1.4	mA	2.1	mA

featuring

- Full Decoding of Input Logic
- 80-mA Sink Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Logic

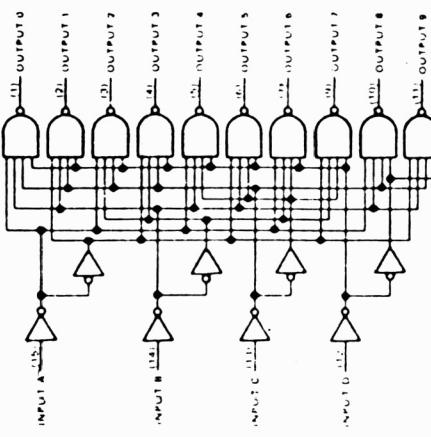
FOR USE AS LAMP, RELAY, OR MOS DRIVERS

JOP N DUAL IN LINE OR
W FLAT PACKAGE (TOP VIEW)



-67-

functional block diagram



PARAMETER	TEST CONDITIONS ¹	MIN	TYP.	MAX	UNIT
High-level input voltage	V _{CC} - MIN, I _I = 12 mA	0.8	V	1.5	V
One-level input voltage	V _{CC} - MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = 400 μ A	2.4	V	3.4	V
High-level output voltage	V _{CC} - MIN, V _{OH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 400 μ A	0.7	V	0.4	V
One-level output voltage	V _{CC} - MIN, V _{OH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 400 μ A	1	mA	1	mA
Input current at maximum input voltage	V _{CC} - MAX, V _I = 5.5 V	20	mA	20	mA
High-level input current	V _{CC} - MAX, V _I = 4 V	0.8	mA	0.8	mA
One-level input current	V _{CC} - MAX, V _I = 0.4 V	9	mA	20	mA
Short-circuit output current ²	V _{CC} - MAX, V _I = 0.4 V	14	mA	27	mA
Supply Current	See Note 2	1.4	mA	2.1	mA

Note 1: Ratings shown as MIN or MAX, use the appropriate values for SN5445 and SN7445 decoders/drivers, using one input at a time. The value of V_{CC} = 5 V, T_A = 25°C.

Note 2: When one output should be shorted at a time, V_{CC} is measured with all inputs grounded and outputs open.

Characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER

TEST CONDITIONS	MIN	TYP.	MAX	UNIT
Propagation delay time, high-to-low level output from A, B, C, or D through 2 levels of logic	10	44	60	ns
Propagation delay time, high-to-low level output from A, B, C, or D through 3 levels of logic	15	46	70	ns
Propagation delay time, low-to-high level output from A, B, C, and D through 2 levels of logic	34	50	56	ns
Propagation delay time, low-to-high level output from A, B, C, and D through 3 levels of logic	52	70	113	ns

Low circuit and voltage waveforms are shown on page 148.

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters, plus four input buffers designed for use as indicator/relay drivers or as open collector logic circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

description

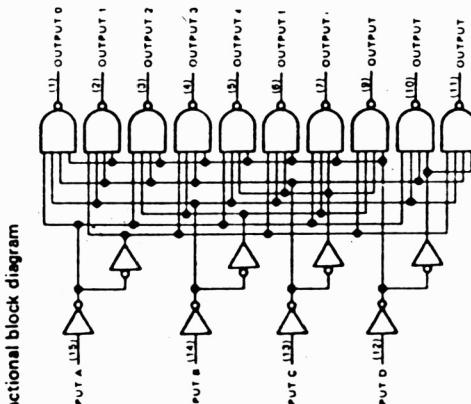
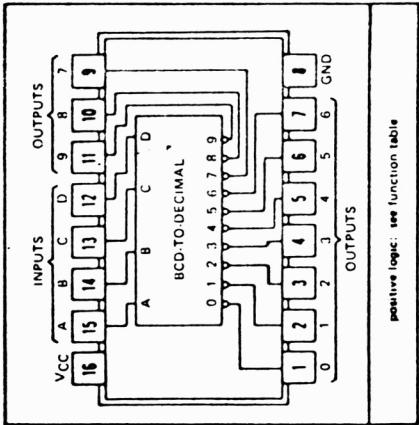
TTI MSI

TYPES SN54145, SN74145 BCD-TO-DECIMAL DECODER/DRIVERS

BULLETIN NO. DLS 7211M5, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

J-OR INDUAL IN LINE OR
W FLAT PACKAGE (TOP VIEW)



functional block diagram

INVALID	INPUT A		INPUT B		INPUT C		INPUT D		OUTPUT 0		OUTPUT 1		OUTPUT 2	
	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-pn output transistors designed for use as latching relay drivers or as open-collector logic circuit buffers. Each of the high-breakdown output transistors (15 V) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off state)	1 mA
Operating free air temperature range: SN54145 Circuits	-55°C to 125°C
SN74145 Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

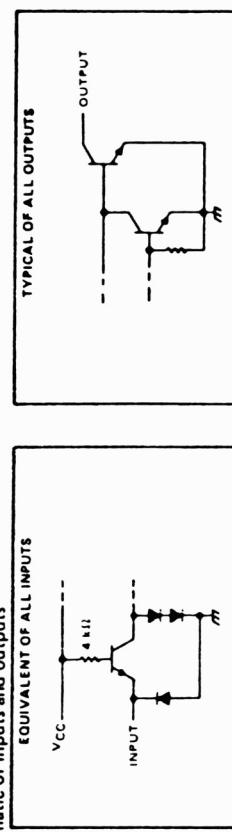
PARAMETER	TEST CONDITIONS ¹		
	MIN	NOM	MAX
V_{IH} — High level input voltage ²	2	5	7 V
V_{IL} — Low level input voltage ²	0.8	0.9	V
V_I — Input clamp voltage ²	-1.5	-1.5	V
$V_{O(H)}$ — On-state output voltage ²	0.5	0.9	1.5 V
$V_{O(L)}$ — Off state output voltage ²	0.4	0.4	V
I_1 — Input current at maximum input voltage ²	15	15	V
I_{IH} — High level input current	1 mA	1 mA	
I_{IL} — Low level input current	40 μA	40 μA	
I_{CC} — Supply current	43 mA	62 mA	70 mA
SN54145	SN54145	SN54145	SN54145
SN74145	SN74145	SN74145	SN74145

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
² All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

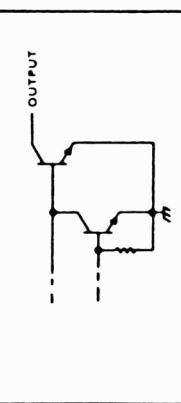
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		
	MIN	NOM	MAX
t_{PLH} — Propagation delay time, low-to-high level output	50 ns	50 ns	
t_{PHL} — Propagation delay time, high-to-low level output	50 ns	50 ns	
NOTE 3: Load circuit and waveforms are shown on page 14II.			
EQUIVALENT OF INPUTS AND OUTPUTS			



TYPICAL OF ALL OUTPUTS



TYPES SN54145, SN74145 BCD-TO-DECIMAL DECODER/DRIVERS

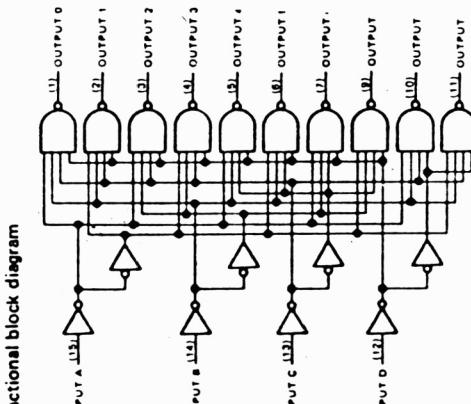
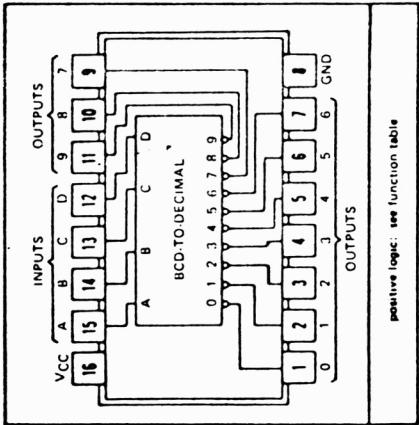
BULLETIN NO. DLS 7211M5, DECEMBER 1972

BCD-TO-DECIMAL DECODER/DRIVERS

BULLETIN NO. DLS 7211M5, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

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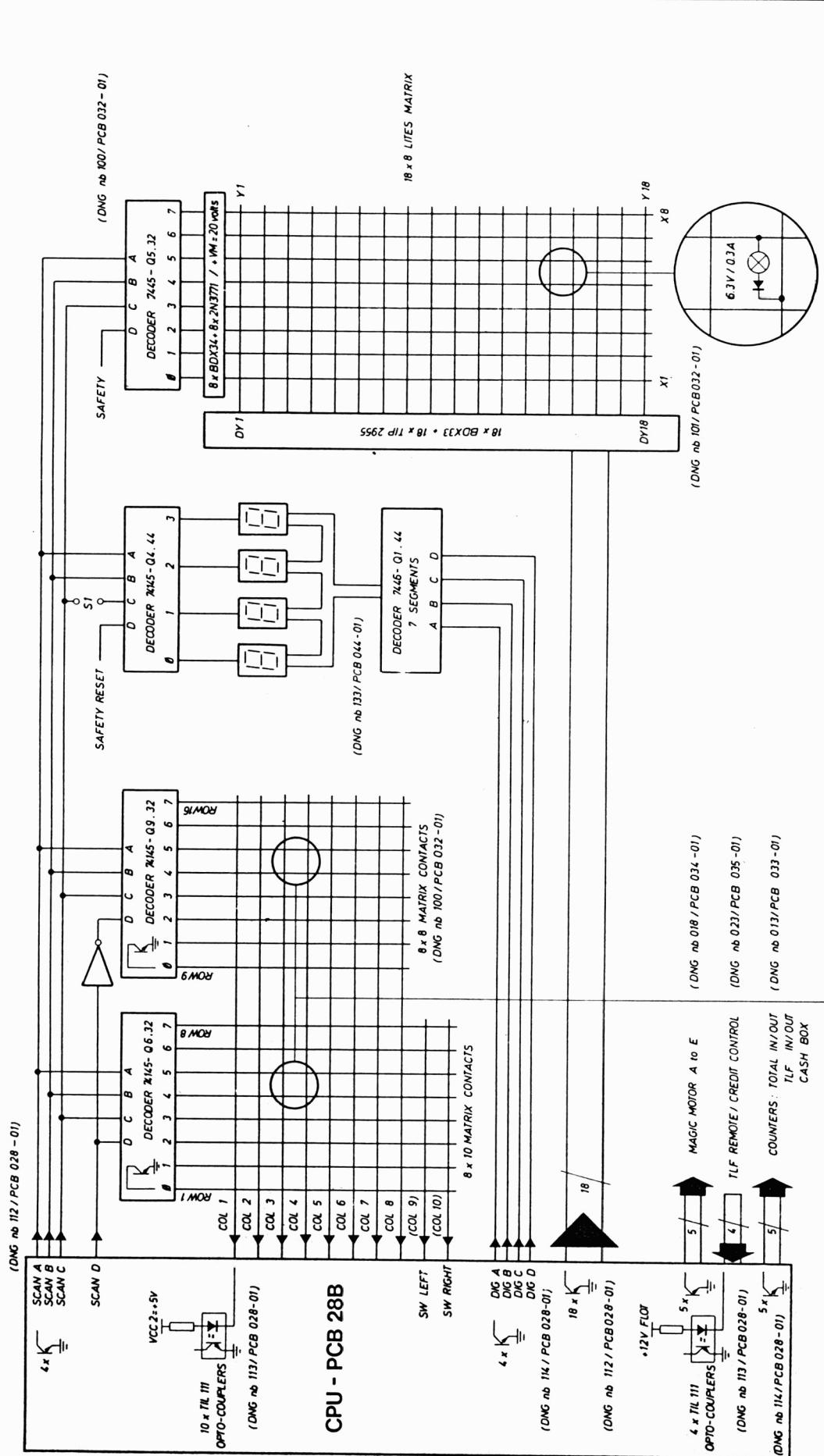
functional block diagram

INVALID	INPUT A		INPUT B		INPUT C		INPUT D		OUTPUT 0		OUTPUT 1		OUTPUT 2	
	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111
1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111	1111

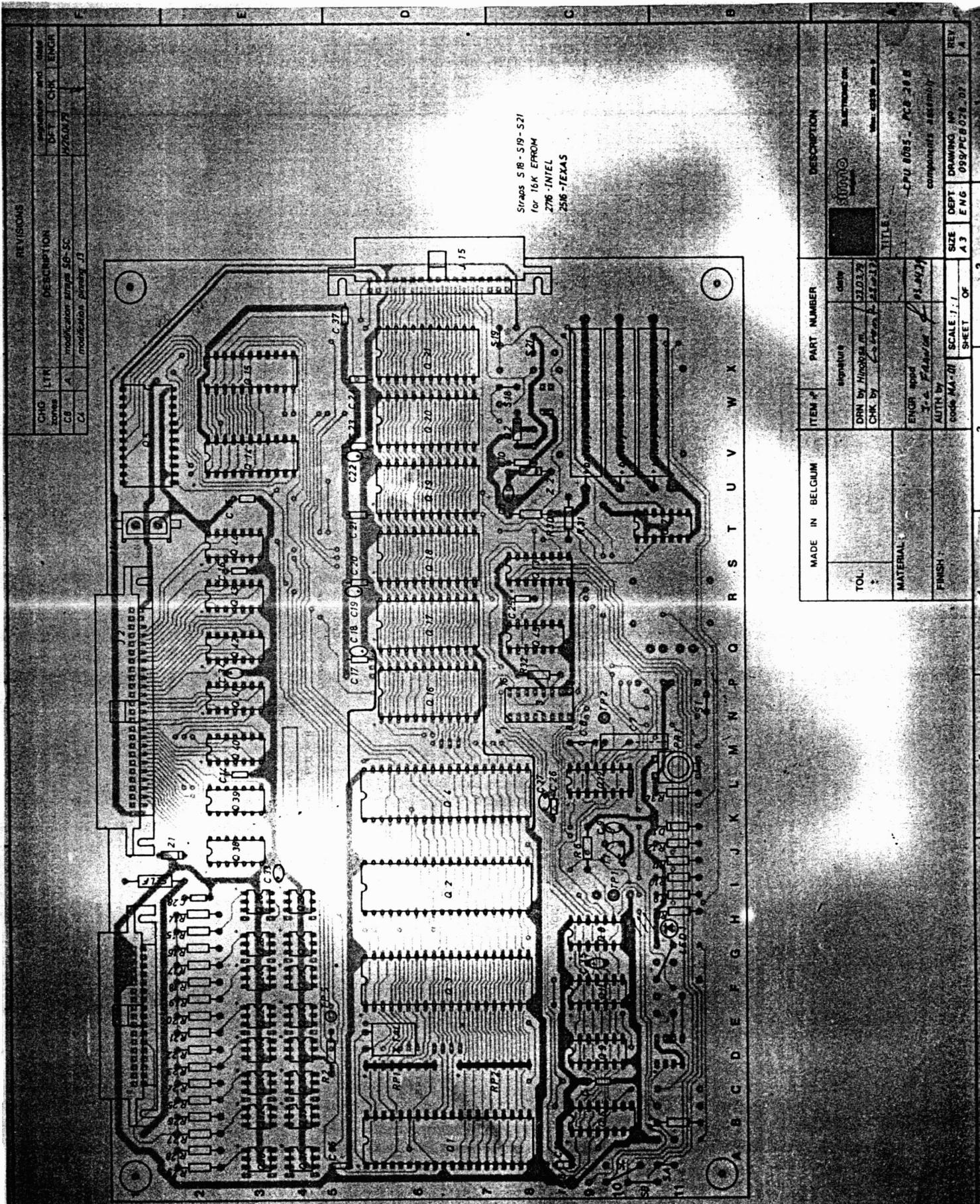
description

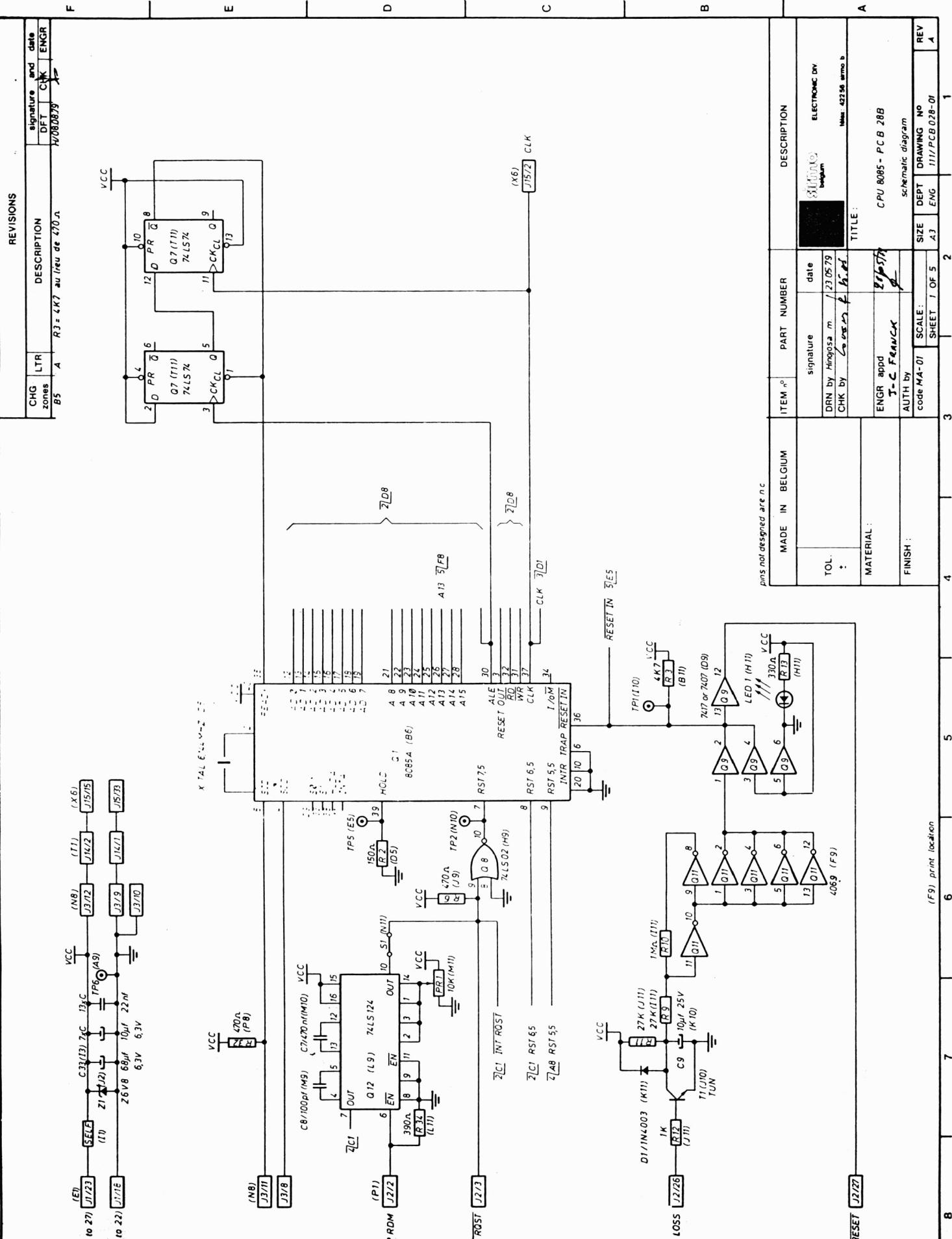
These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-pn output transistors designed for use as latching relay drivers or as open-collector logic circuit buffers. Each of the high-breakdown output transistors (15 V) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

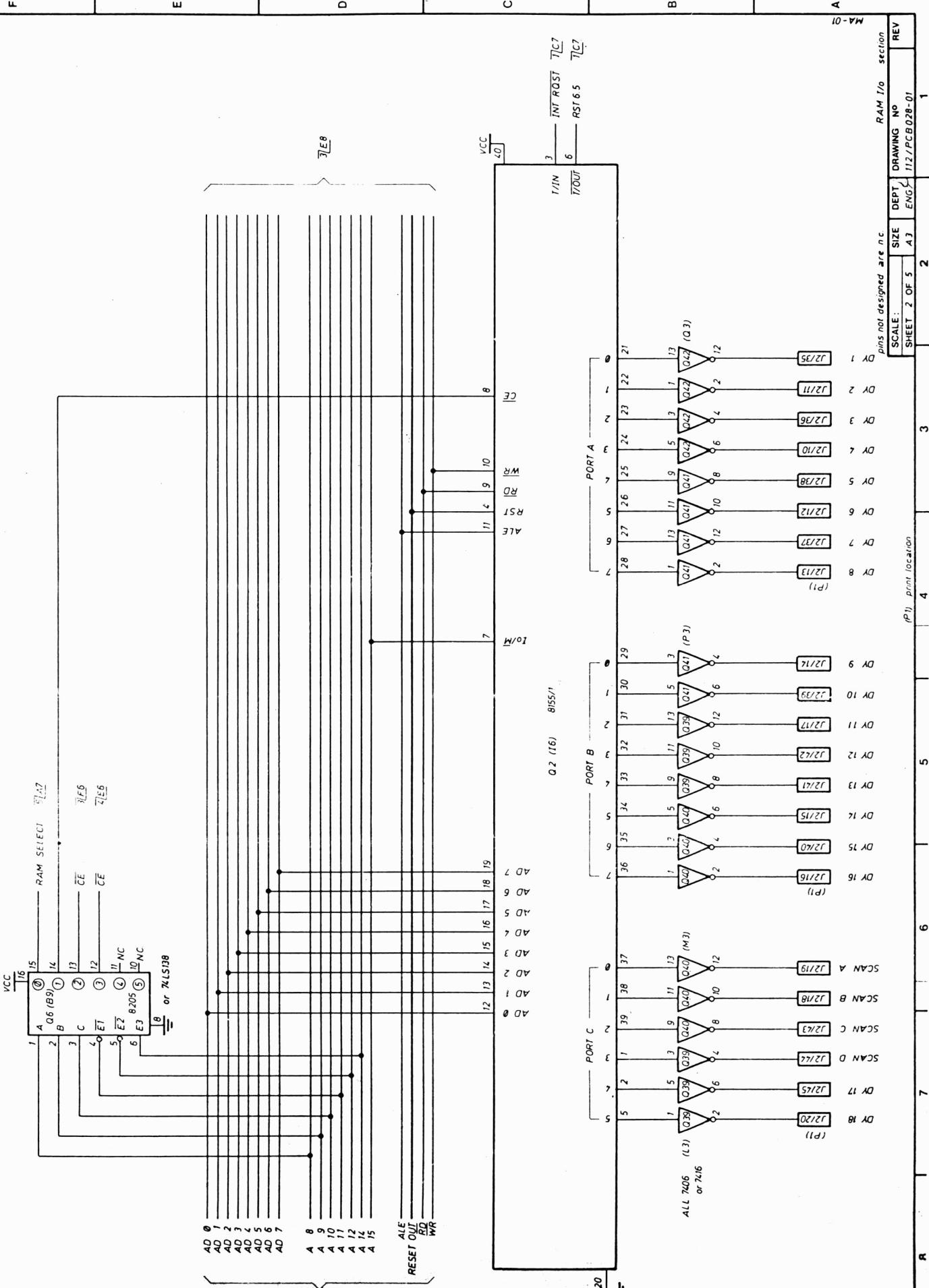
CHAPTER 18 : SCHEMATICS OF THE ELECTRONIC PART

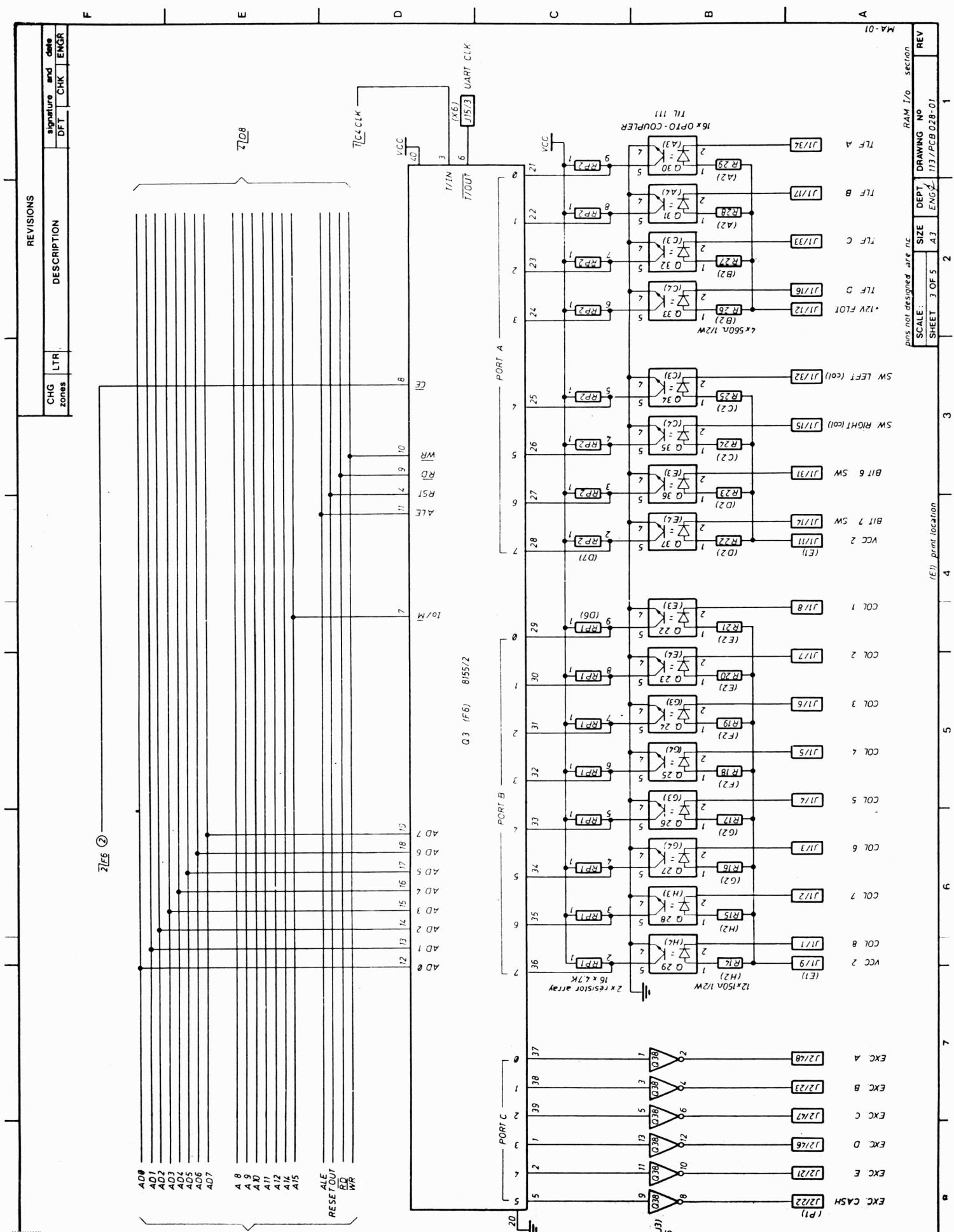


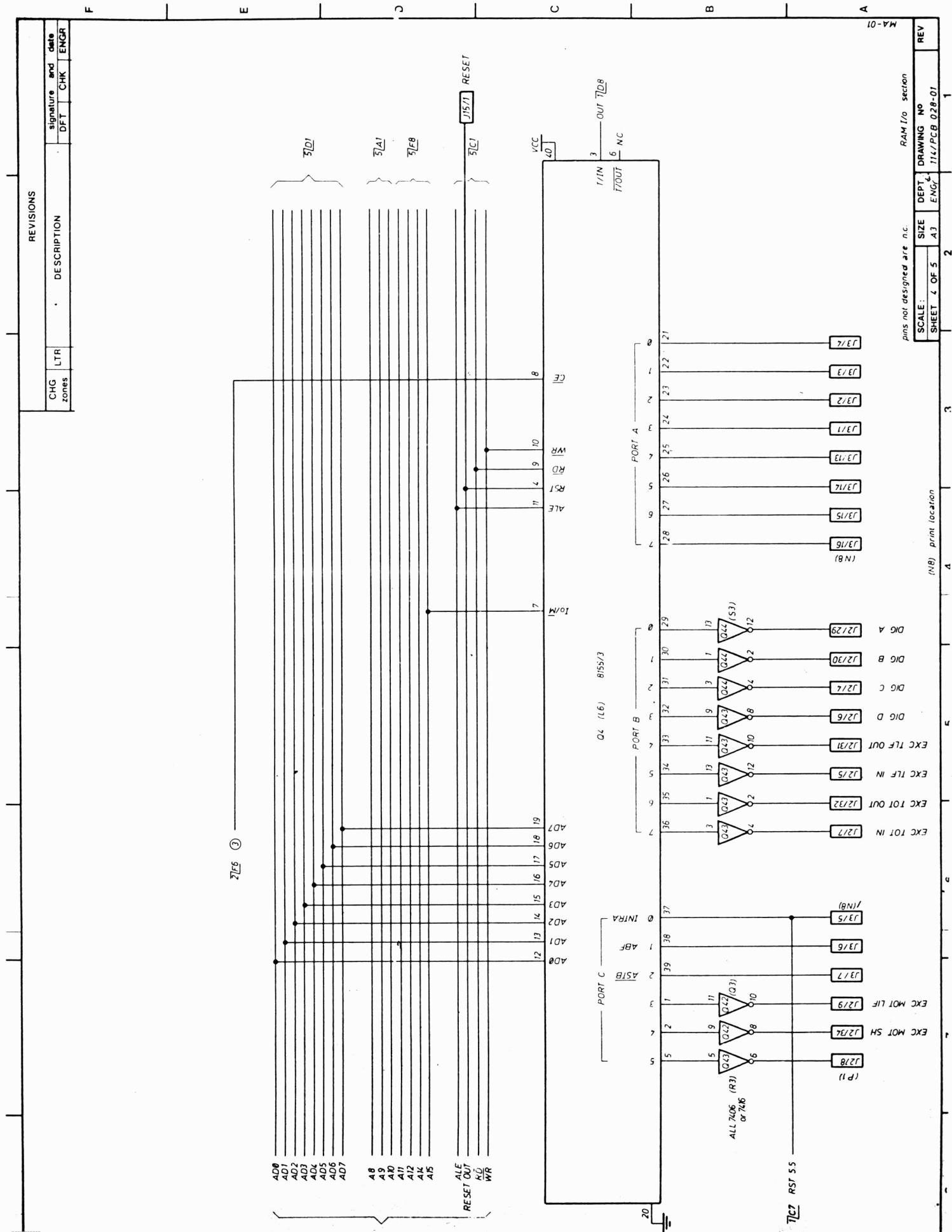
MADE IN BELGIUM		ITEM #	PART NUMBER	DESCRIPTION
TOL. :				
				DRN by Hippo m. L 26.06.79
				CHK by L.C. 26.06.79
				DATE: 42256 mm b
MATERIAL:				TITLE:
				MISS AMERICA schema block
FINISH:				
				ENGR appd J-C FRANCK 21/5/79
				AUTH by
				code MA-01 SCALE: 1:100
				SHEET 1 OF 1
				SIZE: A3 DEPT: NO REV: 00

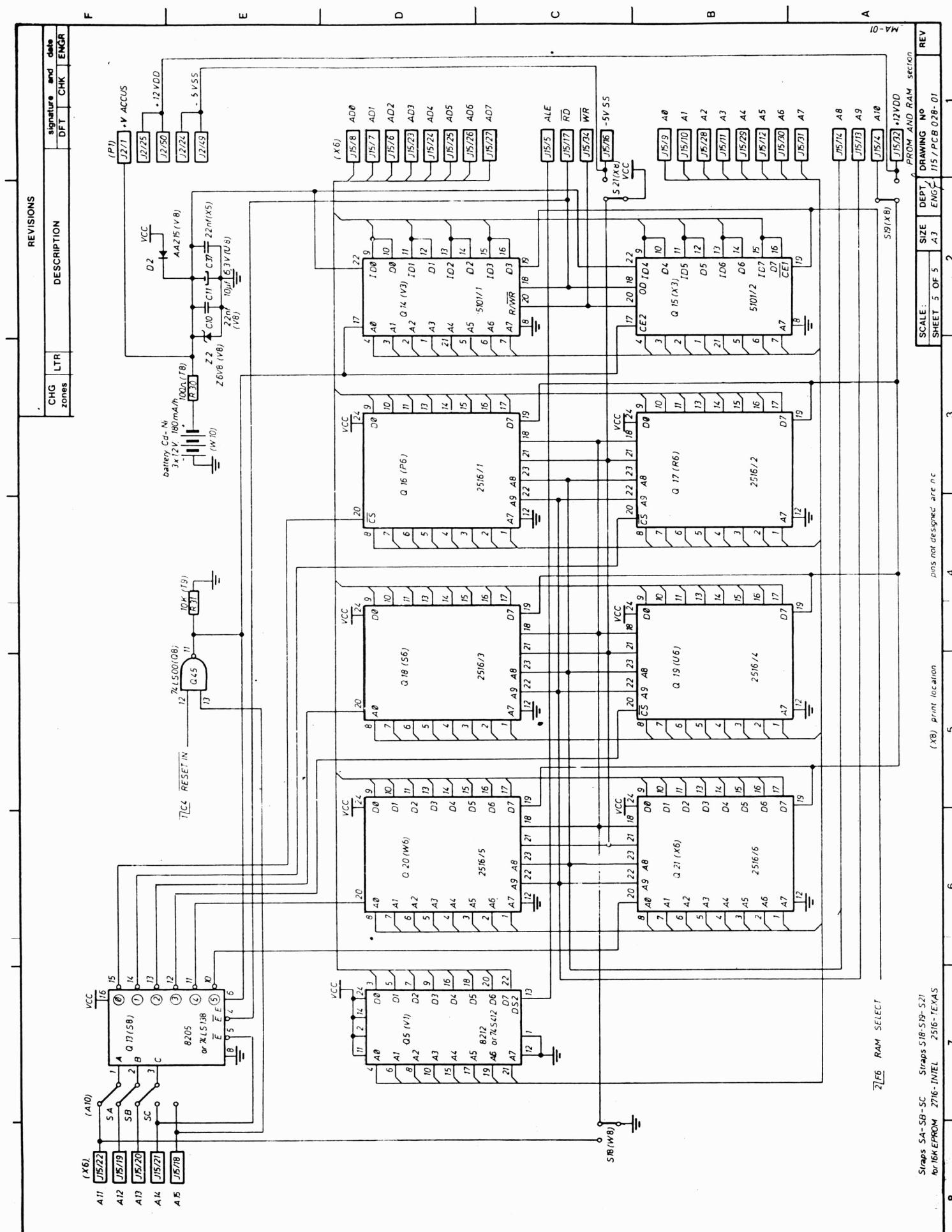


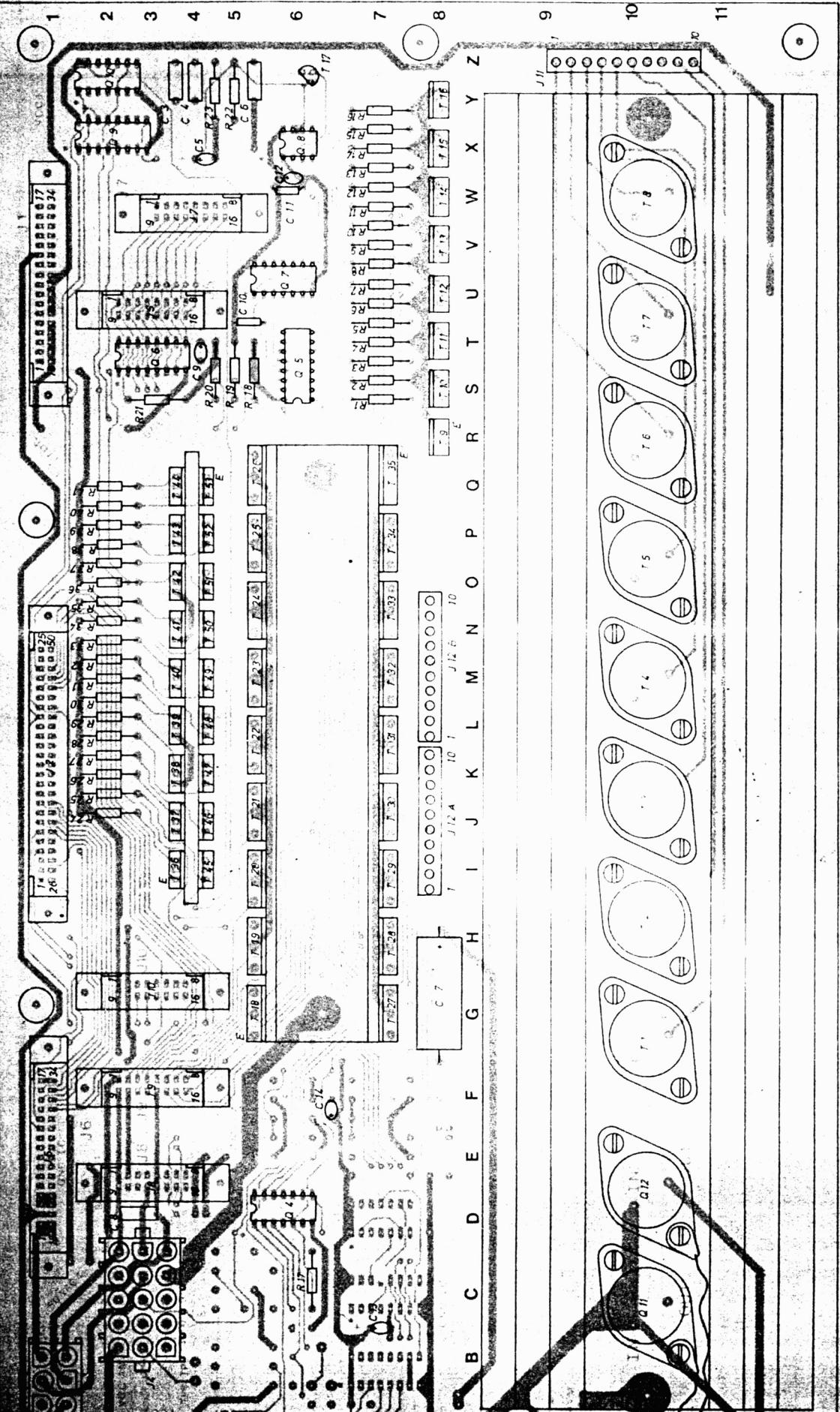




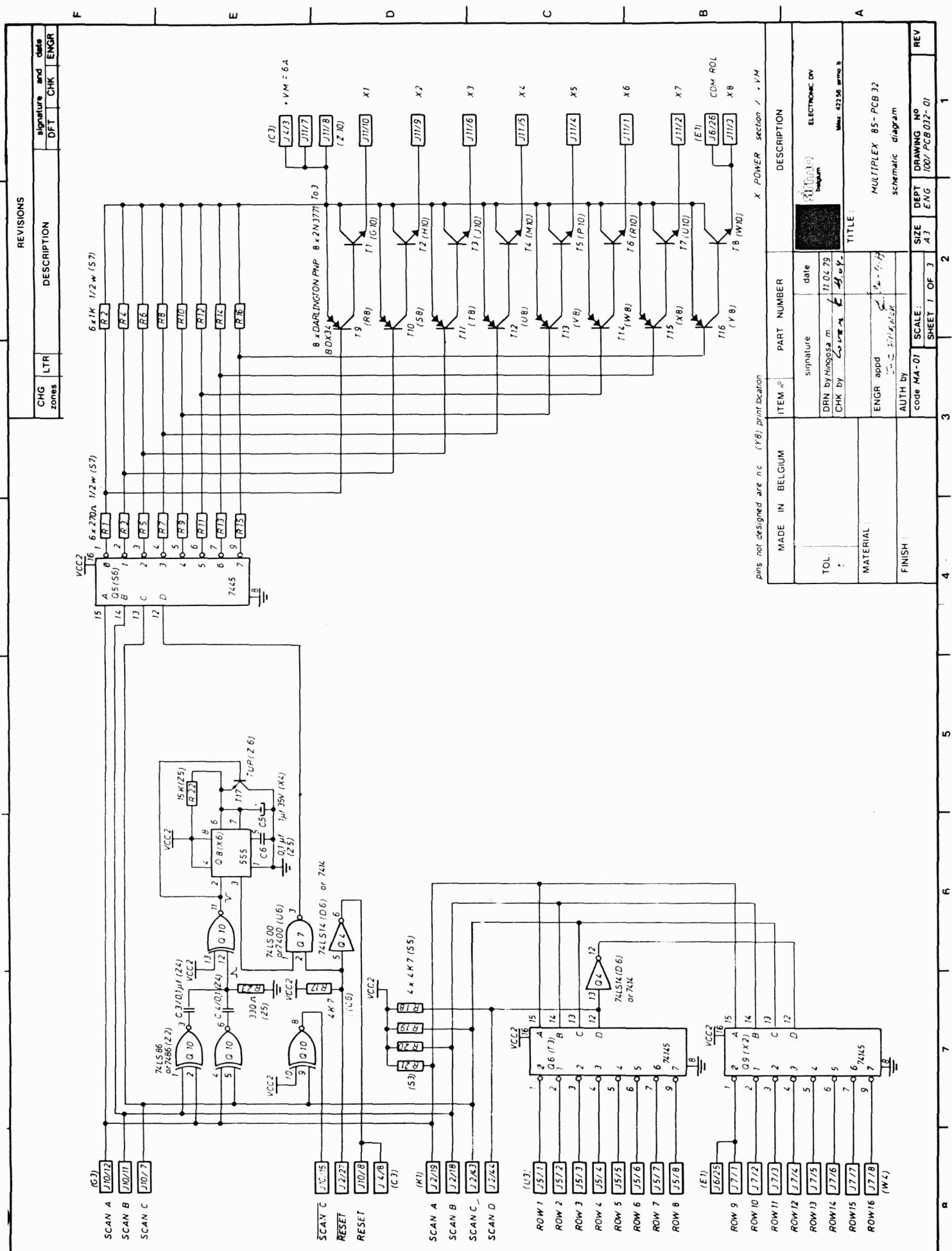


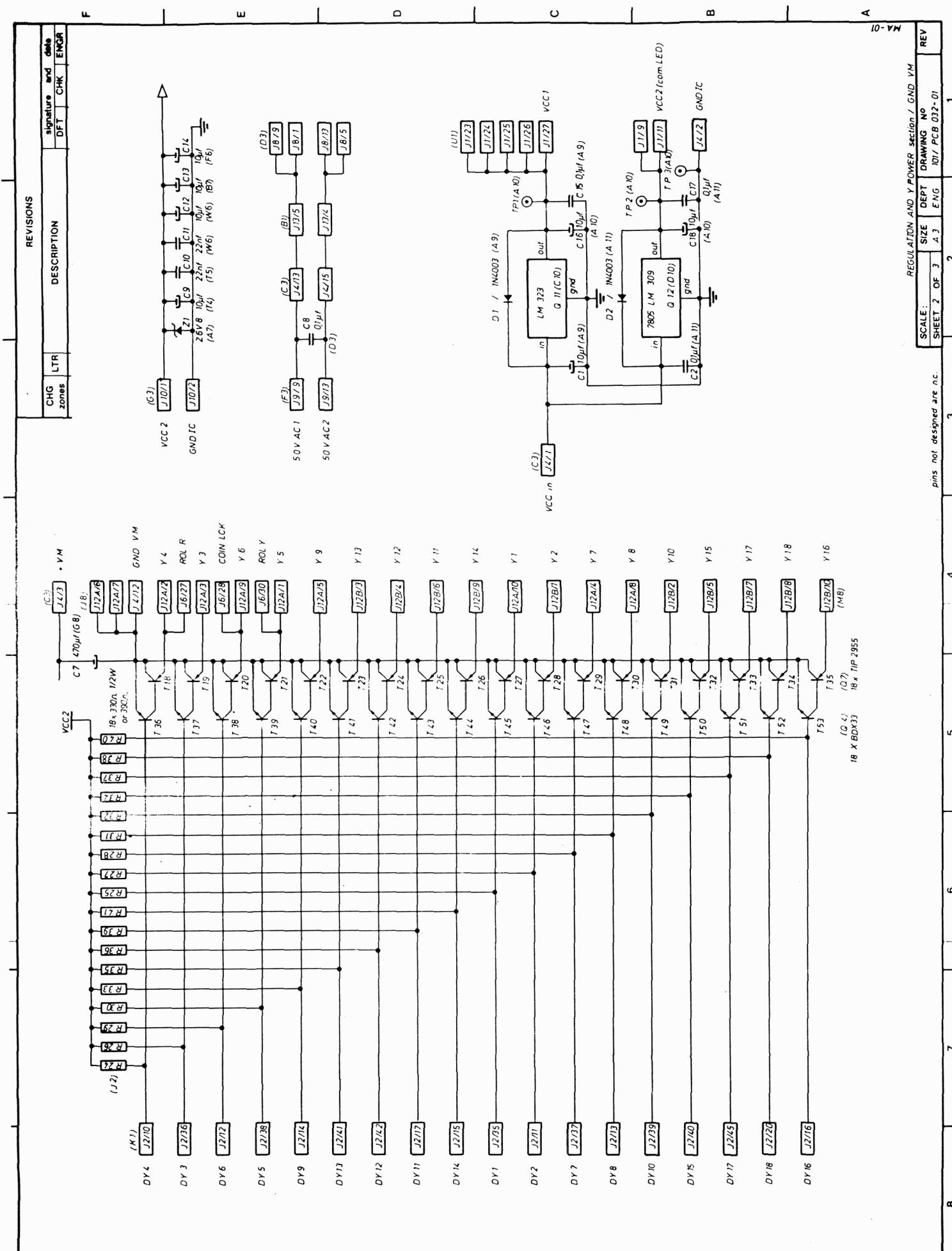


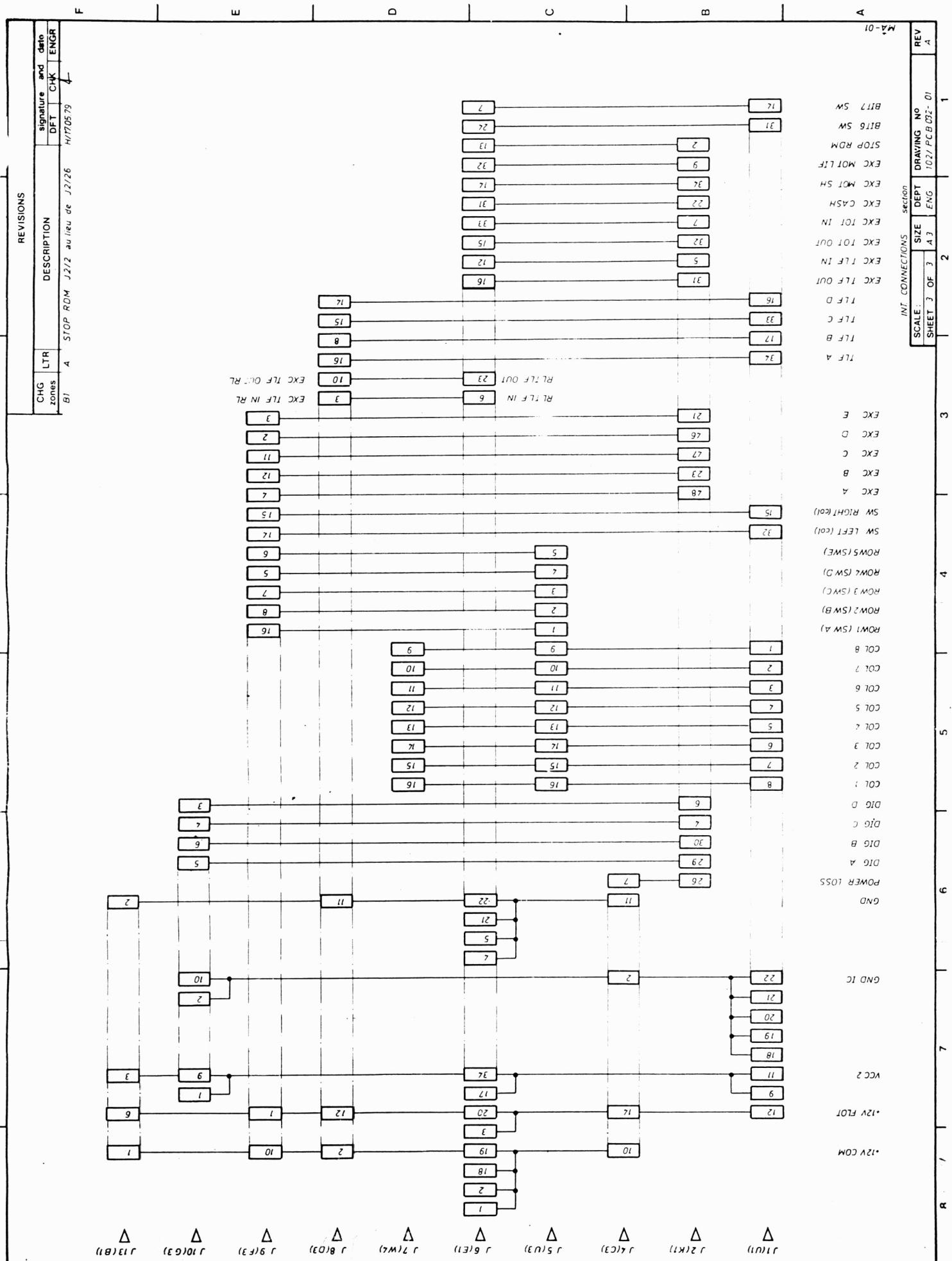


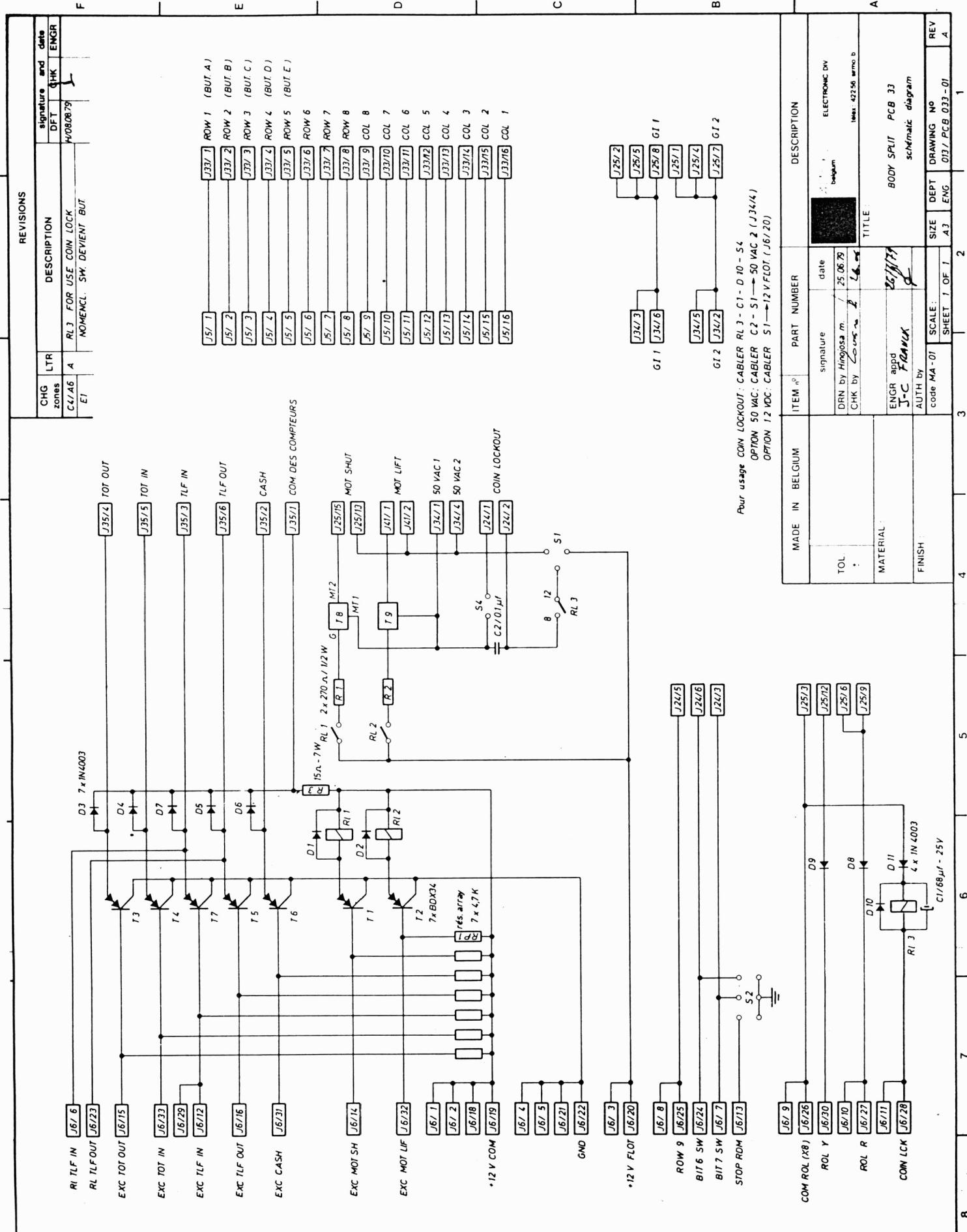


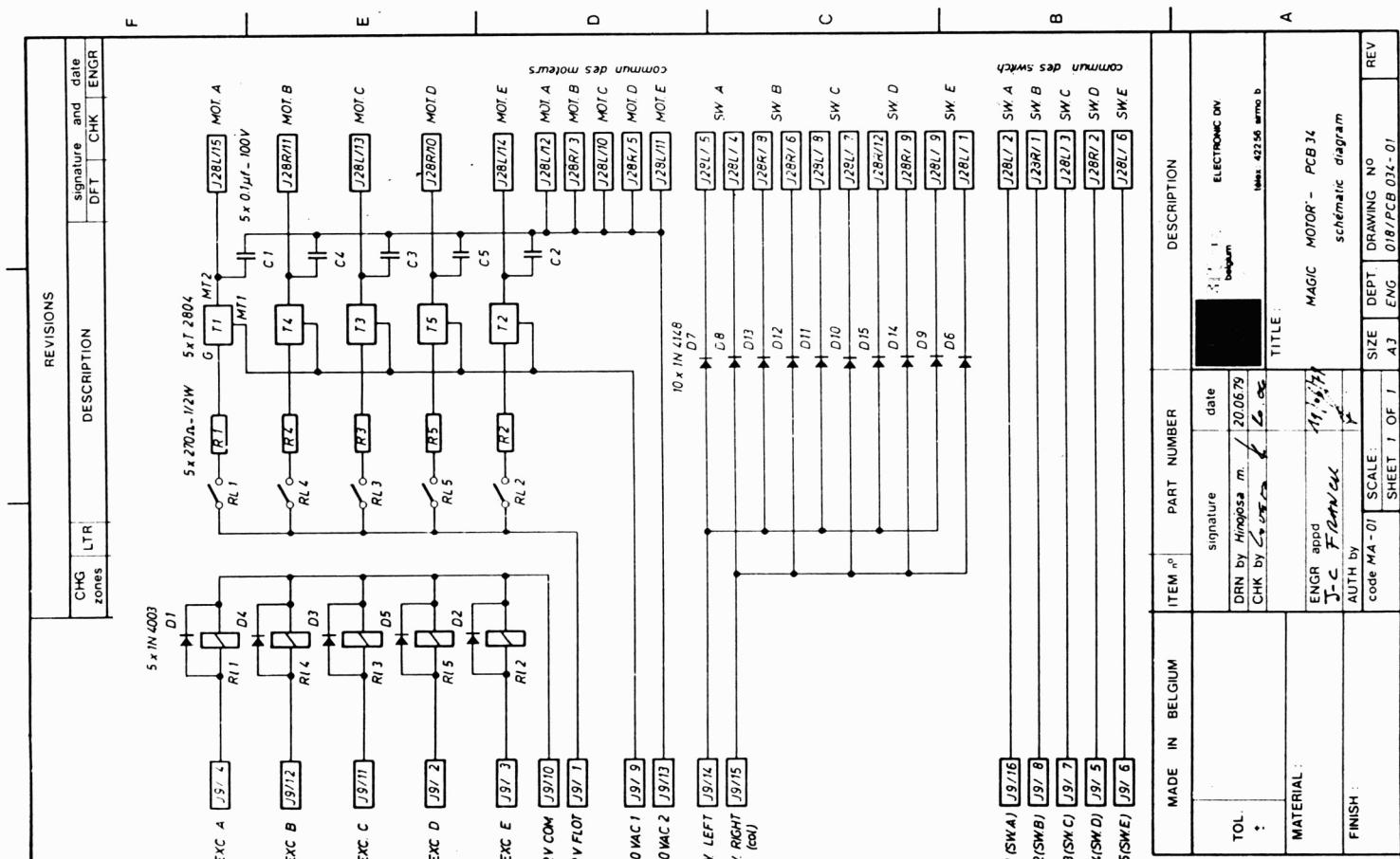
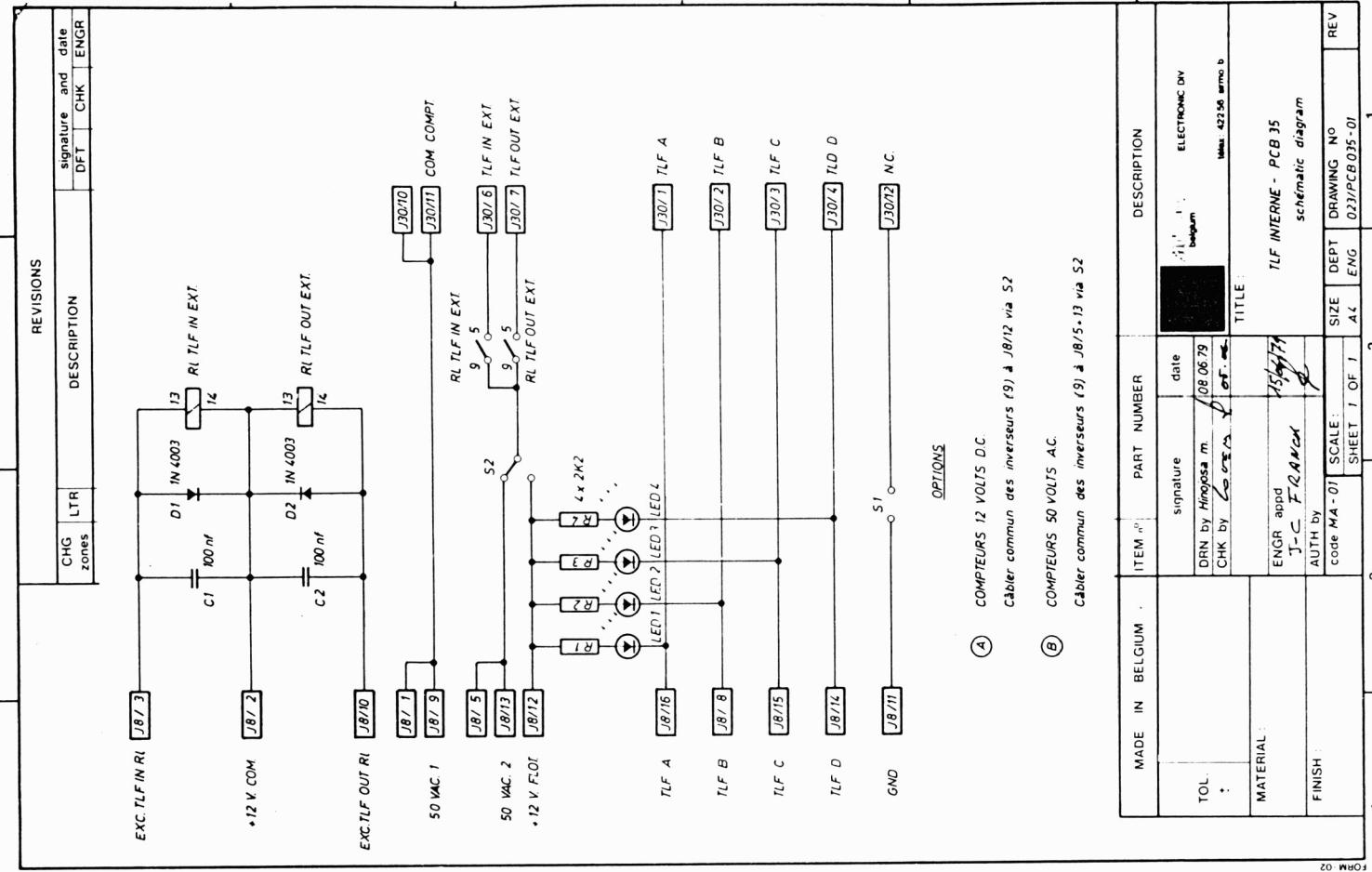
MULTIPLEX 85, PCB 32			
COMPONENTS ASSEMBLY			
TITLE:			
ENGR 8000	signature	date	31/05/79
DRN by Hinoosa m.	J-C. FARAH	03.04.79	ELECTRONIC DEPARTMENT
CHK by			PRINTED BY MURRAY LTD.
MATERIAL:			
TOL:			
FINISH:			
CODE MA-DI	SCALE J : 1	SIZE A 3	DRAWING NO 102/PCB 032-07
		SHEET OF 2	DEPT ENG
			REV 1



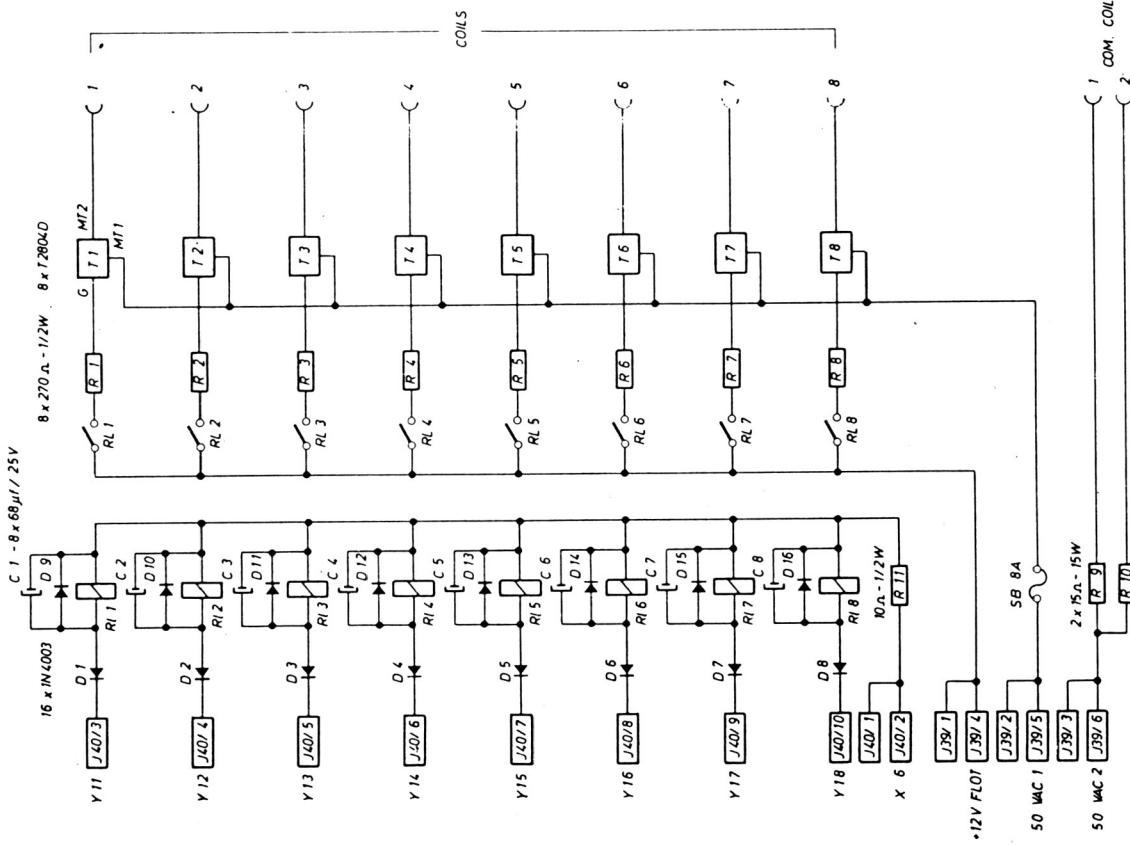








CHG zones	LTR	REVISIONS		signature and date DFT CHK ENGR
		DESCRIPTION		
<u>OPTIONS</u>				
<p>(A) COMPTEURS 12 VOLTS D.C. Câbler S1 - C3 - C4 - D13 - D14</p> <p>(B) COMPTEURS 6 VOLTS D.C. Câbler fil COM. COMPTEUR à J30/12 (COM SW) Pointer J30/12 à J30/10 par une résistance 15Ω/7W Câbler C3 - C4 - D13 - D14</p> <p>(C) COMPTEURS 50 VOLTS A.C. Câbler S1 - R1 - R2 - C1 - C2</p>				
MADE IN BELGIUM	ITEM N°	PART NUMBER	DESCRIPTION	
TOL :	signature	date	TYPICAL DRAWING	
MATERIAL :	DRN by Hingote m.	07.06.79	ELECTRONIC DEV	
FINISH :	CHK by L.	07.06.79	Title: 42756 WMO b	
ENGR and AUTH by		SHEET 1 OF 1		REV
code MA-01		SCALE:	DRAWING NO	028 / PCB 06-01
		SIZE	DEPT	1
		A3	ENG	1



MADE	IN	BELGIUM	ITEM ^o	PART NUMBER	DESCRIPTION
TOL.	:		signature	date	ELECTRONIC DIV baugam
			DRN by <i>Hirogosa m.</i>	<i>27.06.79</i>	Width: 42.56 mm b
			CHK by <i>Z-007-3</i>	<i>R.D.</i>	TITLE:
MATERIAL	ENGR appd	SOUND COLS	DRIVERS - PCB 37	REV	
FINISH:	AUTH by <i>J-C FRANCX</i>	SCALE: code MA-01	DRAWING NO <i>033/PCB 037-01</i>		
		SIZE: SHEET / OF /	DEPT E NG A3		

SOUND COILS	DRIVERS - PCB 37	
	schematic diagram	
DEPT ENG	DRAWING NO	
	033 / PCB 037 - 01	

REVISIONS		signature and date	
CHG	LTR	DFT	ENCR

E D C B A

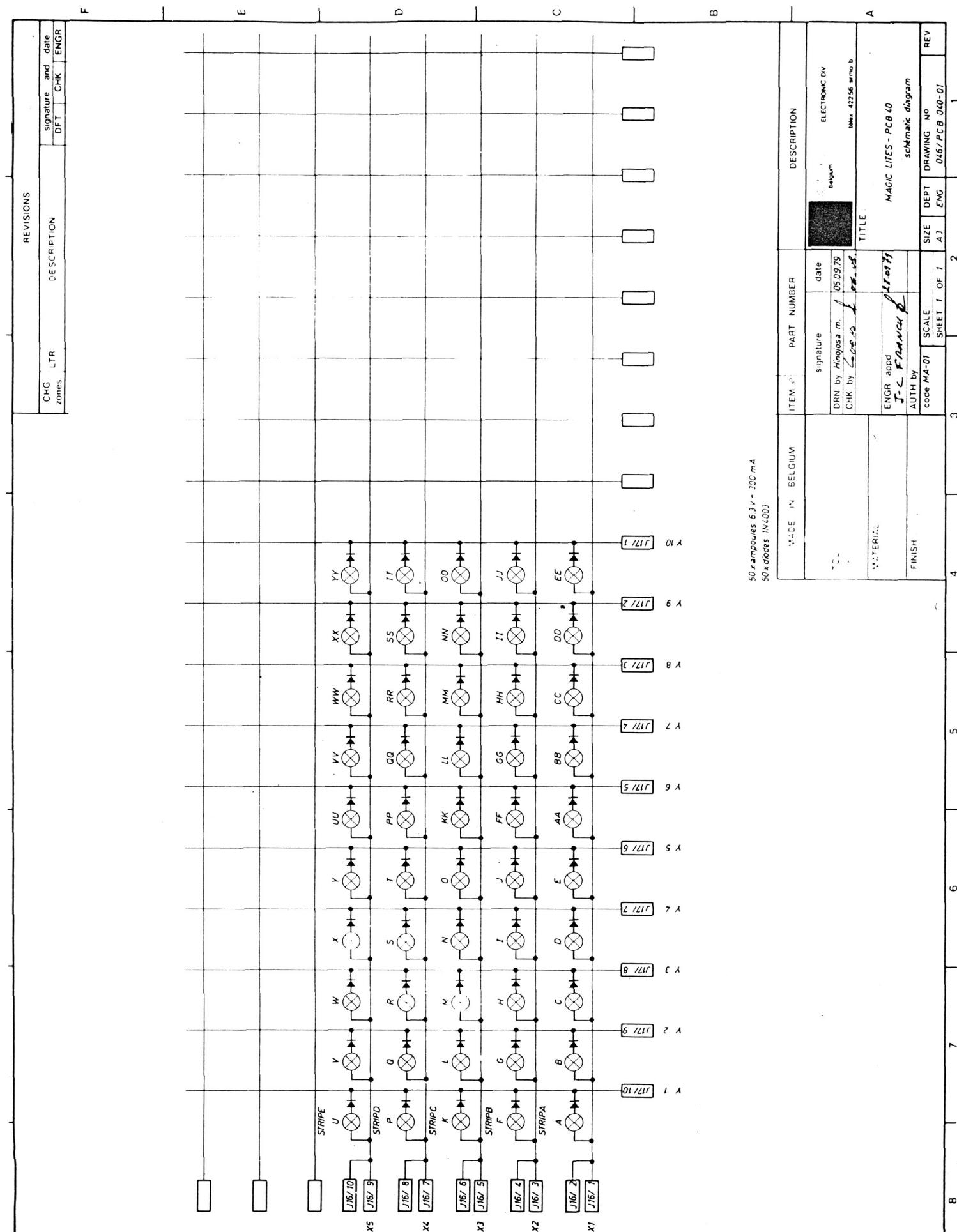
28 x ampoules 6.3V - 300mA
28 x diodes IN4003

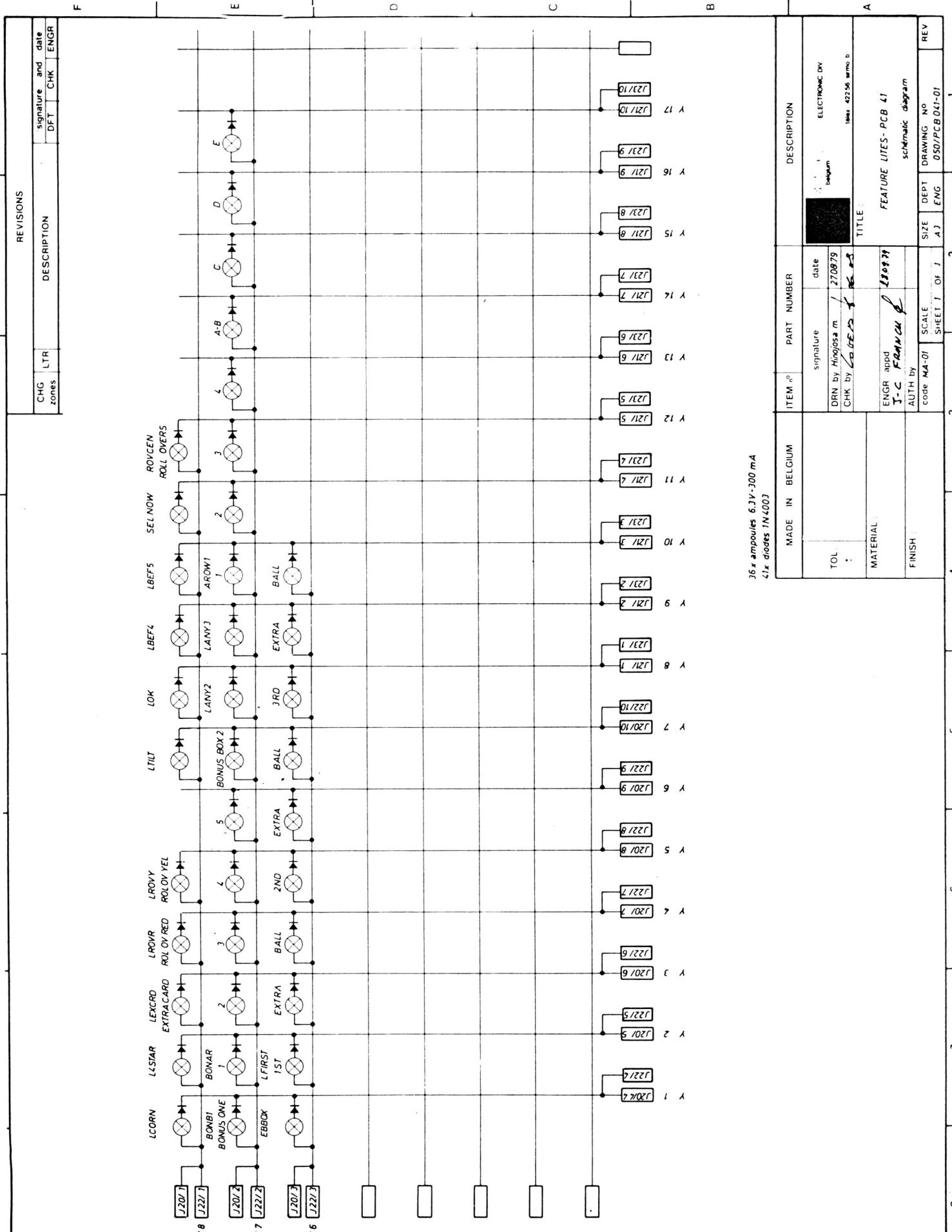
ITEM #	PART NUMBER	DESCRIPTION
MADE IN BELGIUM		
TOL :		
MATERIAL :		
FINISH :		

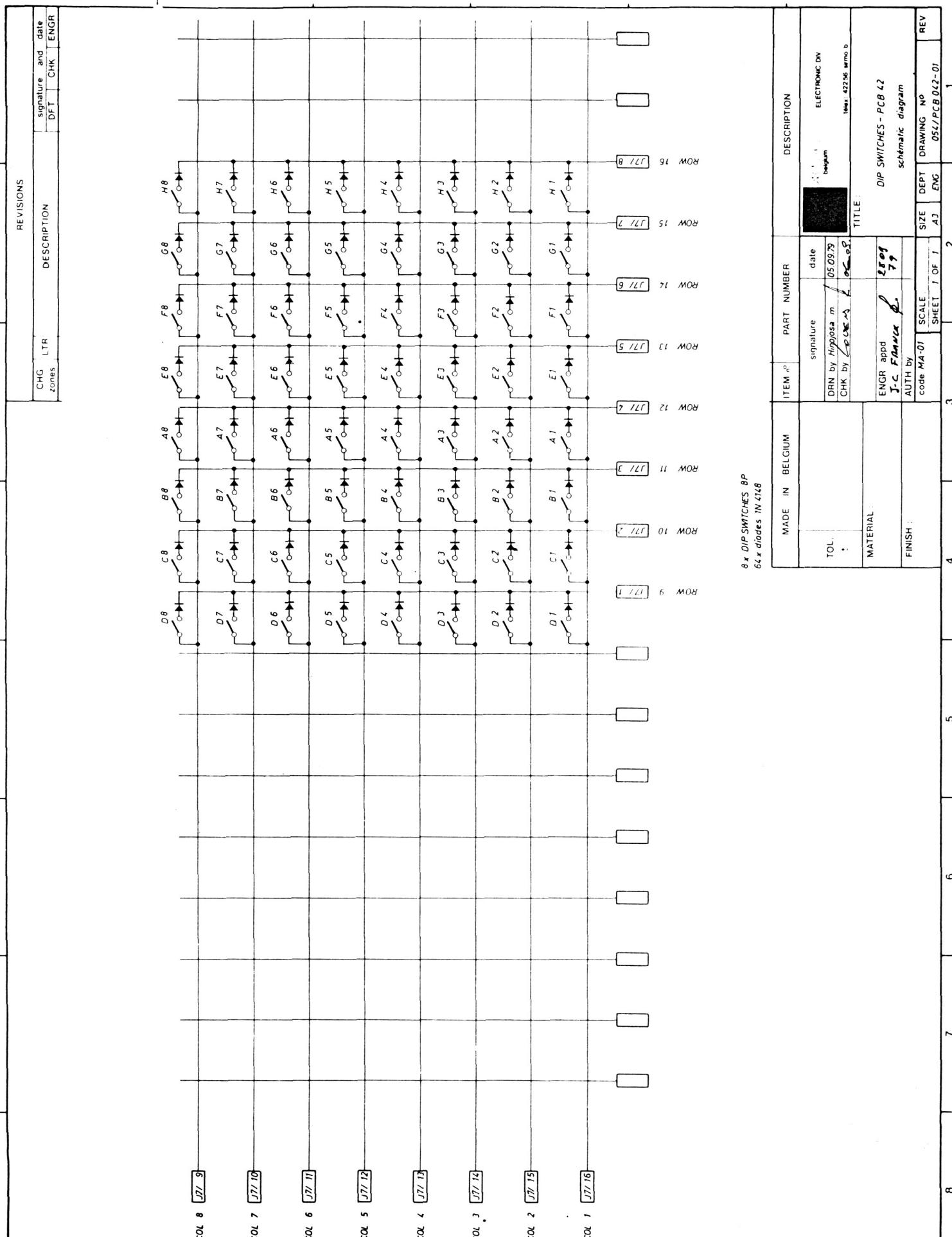
ITEM #	PART NUMBER	DESCRIPTION
J19/3		
J19/8		
J19/9		
J19/0		
LW1/4		
LGR1/4		
LYEL/4		
LRED/4		
V11	J18/1	28 x diodes IN4003
V12	J18/2	
V13	J18/3	
V14	J18/4	
V15	J18/5	
V16	J18/6	
V17	J18/7	
V18	J18/8	
V19	J18/9	
V20	J18/10	

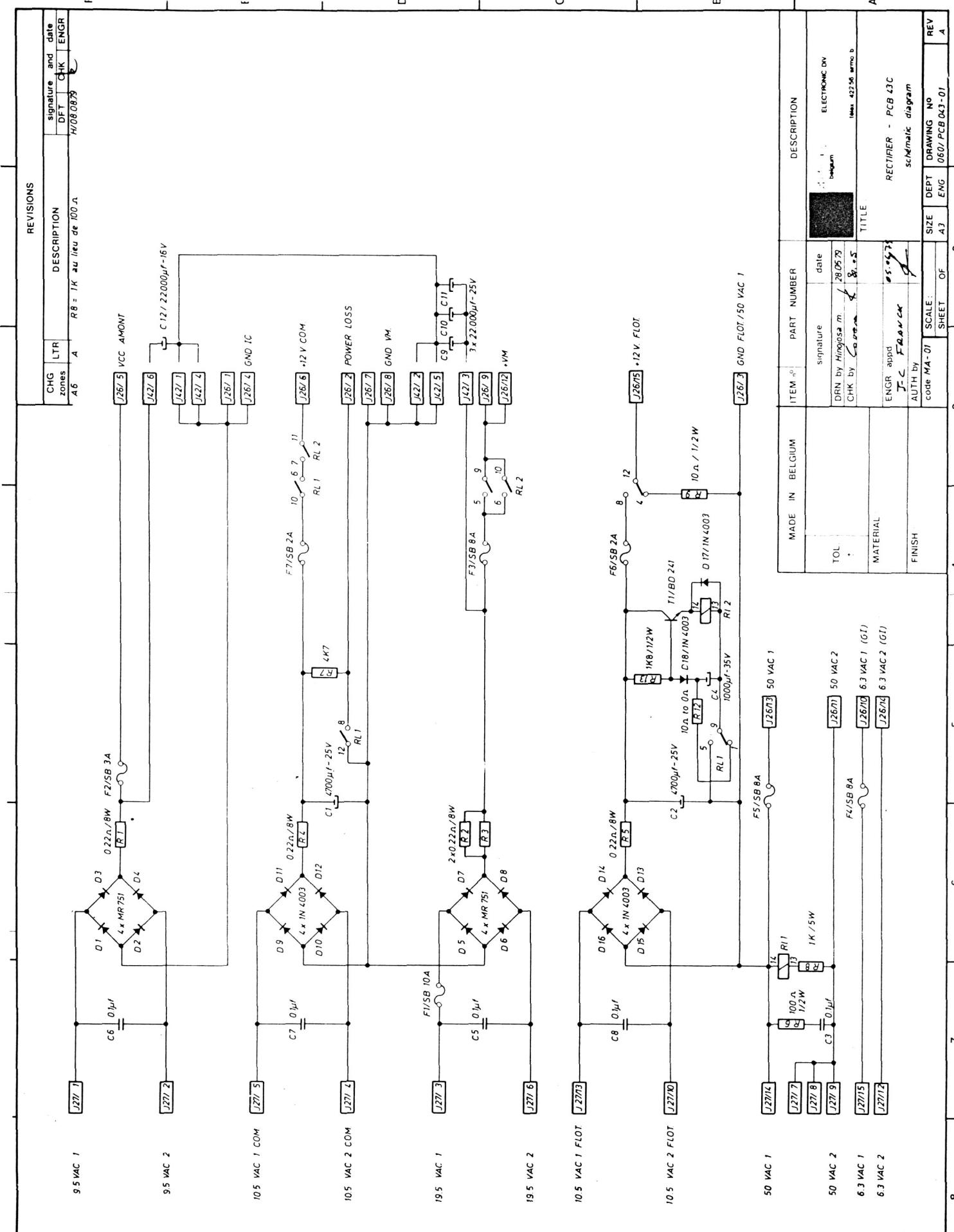
TITLE : SCORE LITES - PCB 39
Schematic diagram

MA-01	SCALE	SIZE	DEPT	DRAWING NO	REV
Sheet 1 of 1	A1				
8	7	5	6	2	1
9	8	4	3	1	



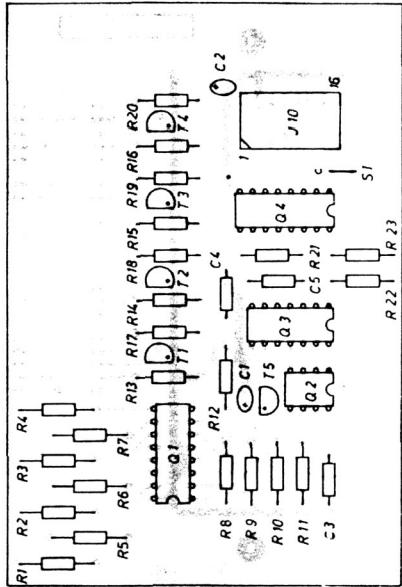
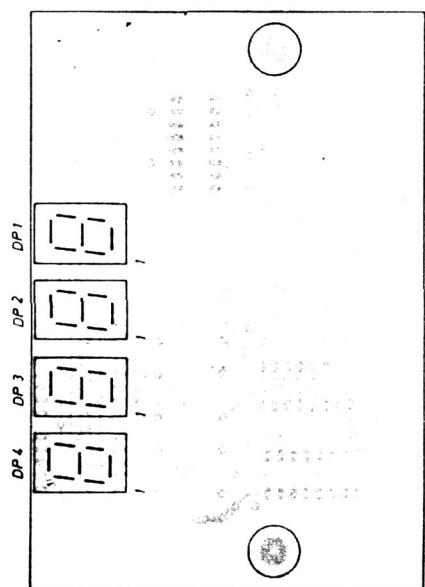






REVISIONS	
CHG zones	LTR

signature and date
DFT CHK ENGR



MADE IN BELGIUM	ITEM #	PART NUMBER	DESCRIPTION
TOL.			PCB UNIT 2
			ELECTRONIC DEVICE
			REF ID: 42256 rev. B
MATERIAL:			
FINISH:			

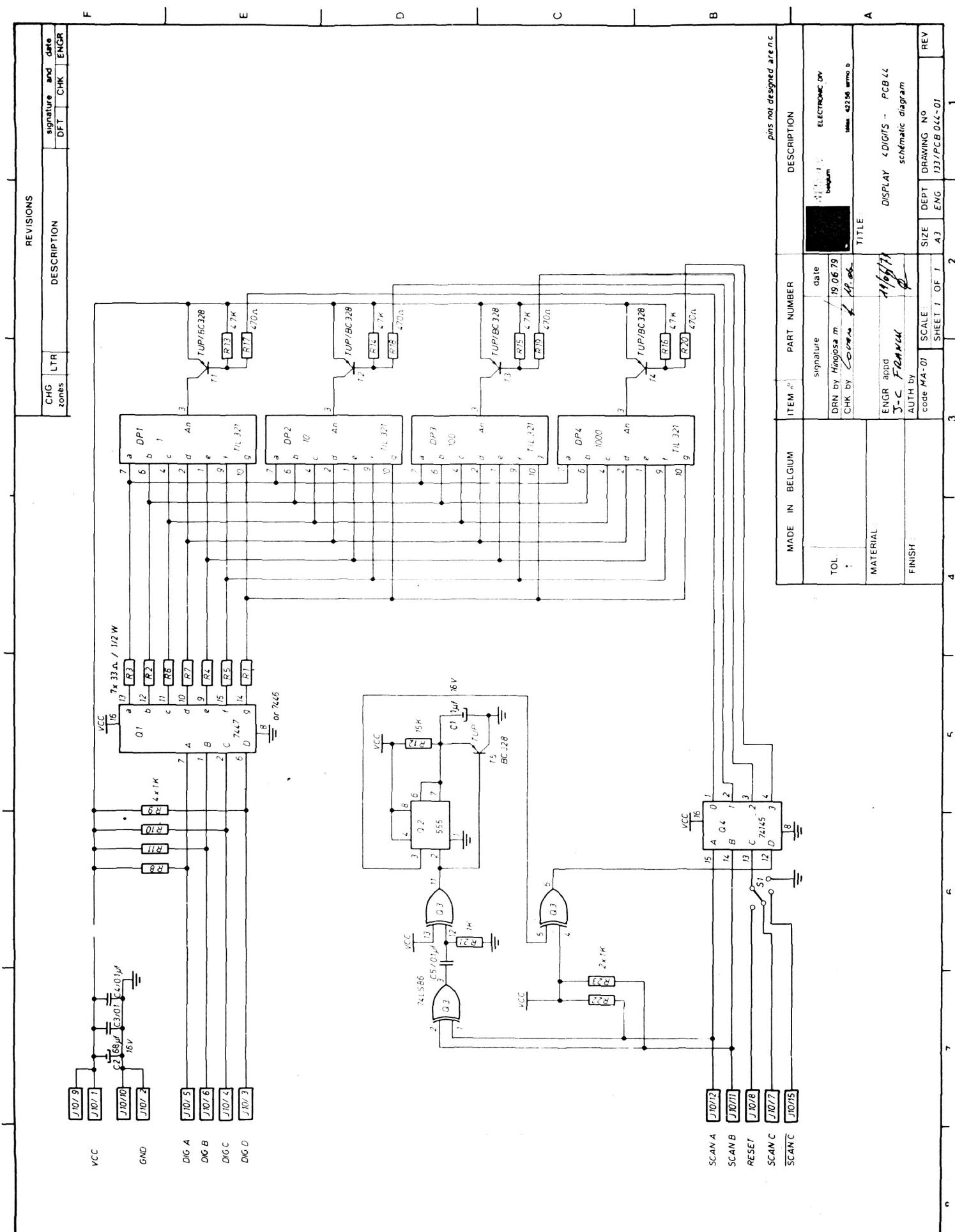
signature date
ORN by Hingose m. 21.06.79
CHK by L. *[Signature]*

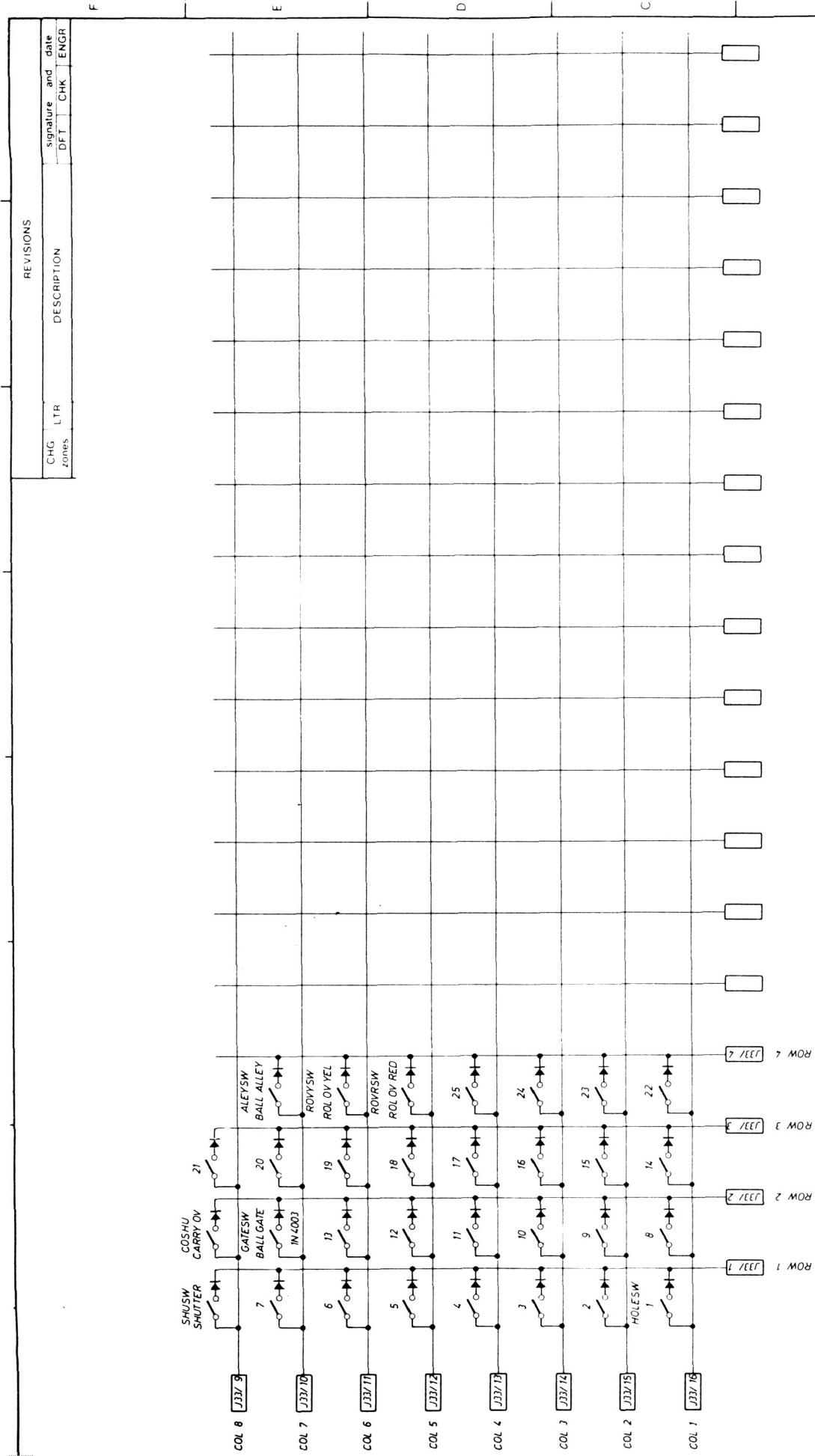
ENGR appd J-C FRANCK
AUTH by *[Signature]*

DISPLAY & DIGITS - PCB 44
COMPONENTS ASSEMBLED

REVIEWED BY: *[Signature]*

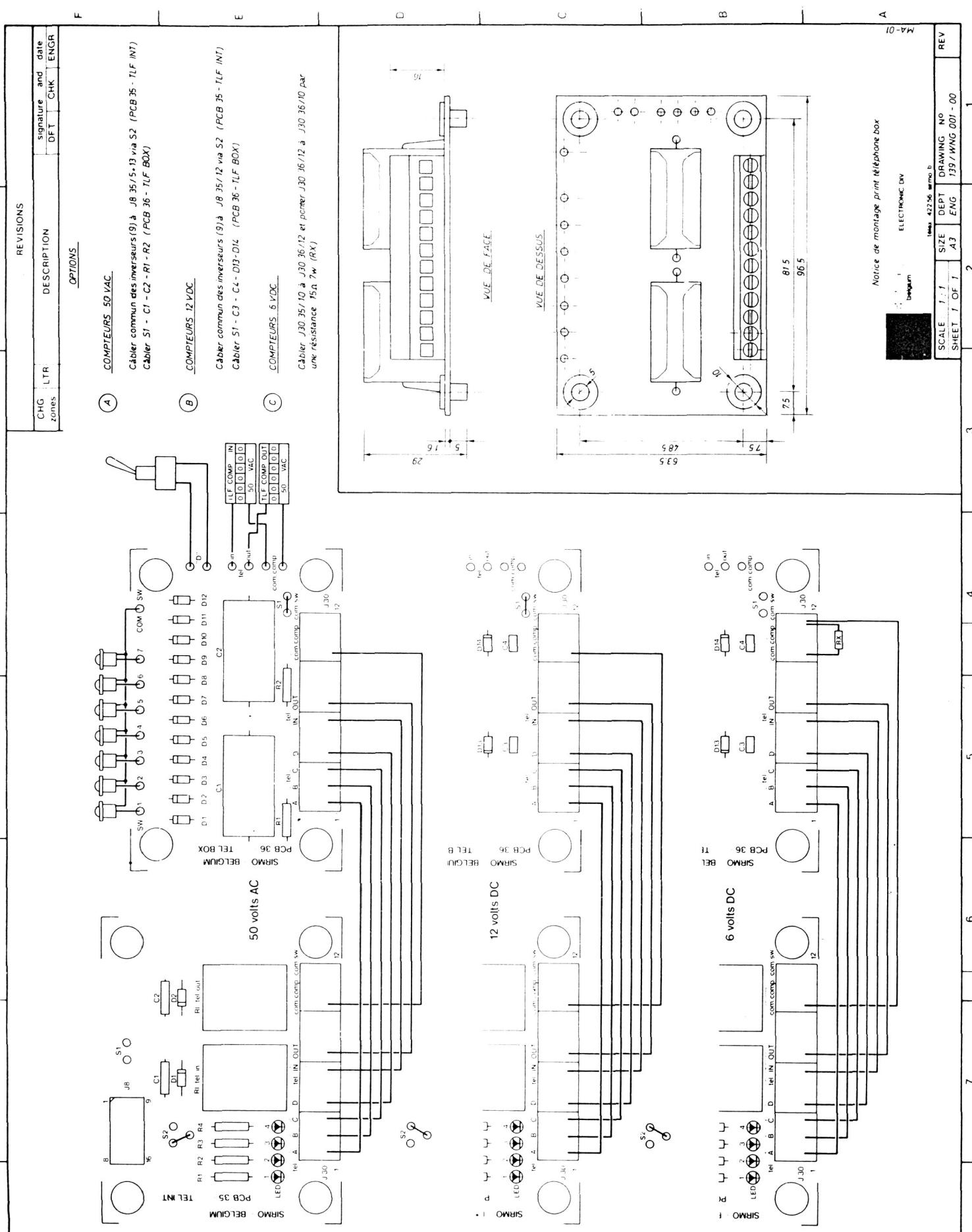
PCB 44
DRAWING NO. 138 / PCB 044-07
SIZE A3 ENG
SHEET 1 OF 1 DEPT A3 REV 0





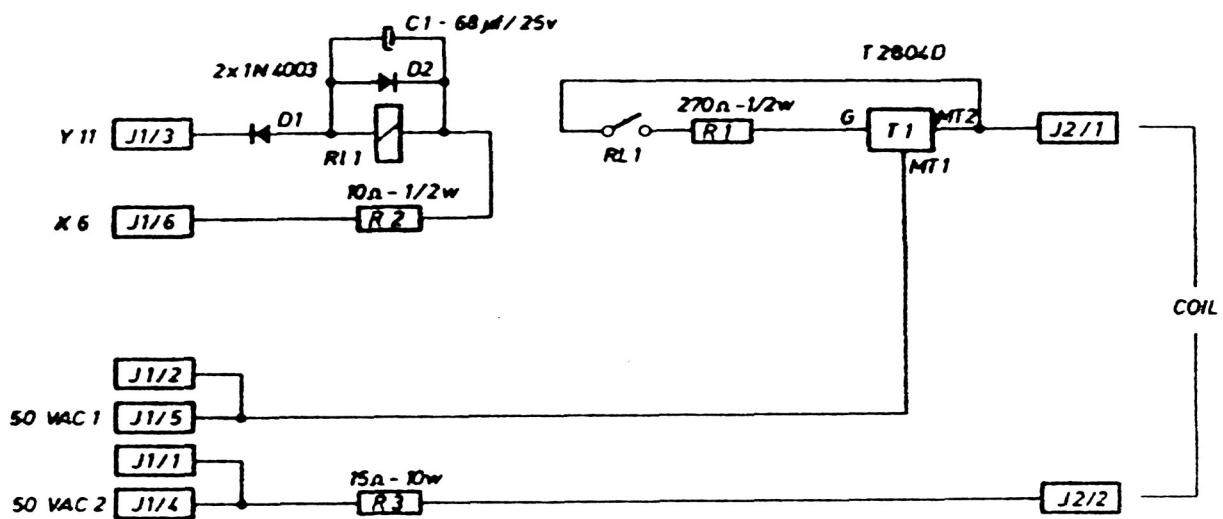
25 x switches NO.
1 x diode 1N 4003
30 x diodes 1N 4168

MADE IN BELGIUM	ITEM NO.	PART NUMBER	DESCRIPTION
TOL :	Signature DAN by Hoogiosa m CHK by C. COOK	Date 03/09/79 Loc. 106-39	Electronic Div board Item: 42756 memo b
MATERIAL:	ENGR appd J.C. Franssen	TITLE: BALL HOLES SWITCHES - PCB 46 schematic diagram (46/1 to 46/5)	
FINISH:	AUTH BY code MA-01	SCALE SHEET 1 OF 1	SIZE A1 DEPT ENG DRAWING NO 163/PCB 06-01 REV. 2



REVISIONS

CHG ZONES	LTR	DESCRIPTION	signature and date
DFT	CHK	ENGR	



MADE IN BELGIUM	ITEM #	PART NUMBER	DESCRIPTION
TOL		signature <i>[Signature]</i> date <i>12.06.60</i>	ELECTRONIC CO. DRAFT
MATERIAL		DRN by <i>[Signature]</i> CHK by <i>[Signature]</i>	Rev. 12246 Ver. 6

TITLE:
SOUND COIL DRIVER - PCB 072
schematic diagram

Miss Americana Triple Bonus

RED SCORES AS FOLLOWS :

5-IN-LINE	:	75	96	125	250	200	325	400	450	600
4-IN-LINE	:	16	24	50	96	128	200	250	325	400
3-IN-LINE	:	4	8	16	32	64	96	125	150	200

YELLOW SCORES AS FOLLOWS :

5-IN-LINE	:	75	96	125	250	200	325	400	450	600
4-IN-LINE	:	16	24	50	96	128	200	250	325	400
3-IN-LINE	:	4	8	16	32	64	96	125	150	200

GREEN SCORES AS FOLLOWS :

5-IN-LINE	:	75	96	125	250	200	325	400	450	600
4-IN-LINE	:	16	24	50	96	128	200	250	325	400
3-IN-LINE	:	4	8	16	32	64	96	125	150	200

WHITE SCORES AS FOLLOWS :

5-IN-LINE	:	75	96	125	250	200	325	400	450	600
4-IN-LINE	:	16	24	50	96	128	200	250	325	400
3-IN-LINE	:	4	8	16	32	64	96	125	150	200

ONLY THE HIGHEST COMBINATION IS REGISTERED